18 drwg. 770-101

Docket: 0756-1603
Date: April 30, 1997

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

REQUEST FOR FILING

[ ] Continuation)
) application under 37 CFR 1.60 (Rule 60)
[X] Divisional)

of pending prior application of

Applicant(s): Shunpei YAMAZAKI, Akira MASE and Toshiji HAMATANI
Serial No.: 08/504,225 Group Art Unit: 2503
Filed: July 19, 1995 Examiner: I. Soward
For: SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

To effect the above-requested filing today:

1. [X] Attached is a true copy of the prior application as filed, including
[X] Specification and claims as originally filed;
[X] Declaration or Oath as originally filed;
[X] 18 Sheet(s) of drawings (Figs. 1-14)
[X] Formal [ ] Informal

2. [ ] Transfer the drawings from the prior application to this application and abandon said prior application as of the filing date accorded this application.

3. [X] Priority is hereby claimed under Rule 55 and 35 USC 119 based on prior foreign application(s) No(s): 3-65418 and 3-135569 filed in (country) JAPAN on (date) March 6, 1991 and May 11, 1991, respectively.

a. [ ] Certified copy(s) attached.
[X] Certified copy(s) already filed on June 24, 1992 in prior United States Serial No. 07/846,164, filed on March 5, 1992.

4. [X] The prior application is assigned to Semiconductor Energy Laboratory Co., Ltd..

5. [X] The Power of Attorney in the prior application is to:

Daniel W. Sixbey, Reg. No. 20,932
Stuart J. Friedman, Reg. No. 24,312
Charles M. Leedom, Jr., Reg. No. 26,477
Gerald J. Ferguson, Jr., Reg. No. 23,016
David S. Safran, Reg. No. 27,997
Thomas W. Cole, Reg. No. 28,290

a. [X] The Power appears in the original papers of the prior application.
b. [ ] Since the Power does not appear in the original papers of the prior application, a copy of the Power is enclosed herewith.

6. [X] Address all future communications to:

Gerald J. Ferguson, Jr.
SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
2010 Corporate Ridge, Suite 600
McLean, Virginia 22102

7. [X] Amend the specification by inserting before the first line the sentence -- This is a Divisional application of Serial No. 08/504,225, filed July 19, 1995, which is a divisional application of Serial No. 08/147,580, filed November 5, 1993, now U.S. Patent No. 5,474,945, which in turn is a divisional application of Serial No. 07/846,164, filed March 5, 1992, now U.S. Patent No. 5,289,030.--

8. [X] Cancel claims 2-22.
(DO NOT CANCEL ALL CLAIMS)

9. [ ] Status as a Small Entity is requested. Executed Small Entity Declaration(s)
[ ] is/are attached.
[ ] was/were filed in prior application on _____
_____.

10. [X] The filing fee is calculated below:

Claims as originally filed, less any claims above cancelled.

	No. Filed	No. Extra	Rate	Fee
Basic Fee				$770.00
Total Claims	1 - 20 =	0	X 11/22	
Independent Claims	1 - 3 =	0	X 40/80	
_____ Multiple Dependent Claim			+ 130/260	
			TOTAL	$770.00

11. [X] Preliminary Amendment attached, to be entered at once.

Total claim fee calculated after amendment:

	No. Filed	No. Extra	Rate	Fee
Total Claims	10 - 20 ** =	0	X 11/22****	$0.00
Independent Claims	1 - 3 *** =	0	X 40/80****	$0.00
			Total Amendment Fee	$0.00
			Total Filing Fee (from Paragraph 10)	$770.00
			TOTAL FEE	$770.00

12. [X] A check in the amount of $770.00 to cover the TOTAL FEE is enclosed.

13. [ ] No fee is enclosed. The filing fee will be submitted later.

14. [X] It is hereby petitioned under 37 CFR 1.136 that the response term in the prior pending application be extended, if necessary, to a date which includes the filing date of the present application, and the Commissioner is hereby authorized to charge any necessary extension fee to Deposit Account No. 19-2380.

15. [X] The Commissioner is hereby authorized to charge fees under 37 CFR 1.16 and 1.17 (except the Issue Fee) which may be required now or

hereafter, or credit any overpayment. to Deposit Account No. 19-2380. A duplicate of this sheet is attached.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

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 Docket: 0756-1603

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of)
Shunpei YAMAZAKI et al.)
Serial No. To be Assigned)
Filed:)
For: SEMICONDUCTOR DEVICE AND)
METHOD FOR FORMING THE SAME)

PRELIMINARY AMENDMENT UNDER 37 CFR §1.607 and
NOTIFICATION OF OTHER AMENDMENTS UNDER 37 §1.607
IN RELATED PATENT APPLICATIONS

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231
Sir:

Please preliminarily amend the subject application in accordance with 37 CFR §1.607.

In the claims:

Please cancel claim 1 and add new claims 23-32 as follows:

--23. A method of manufacturing an active matrix panel in which data signals are supplied to liquid crystal layers through a plurality of thin film transistors arranged in a matrix of pixels, gate lines and data lines being coupled to each thin film transistor, said method comprising the steps of:

forming a semiconductor layer on a substrate;

forming a gate insulating film on said semiconductor layer;

forming a gate electrode above said gate insulating film and a gate line in electrical contact with said gate electrode;

forming a source region and a drain region in said semiconductor layer by adding impurities thereto as donors or acceptors using said gate electrode as a self alignment mask;

simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line and simultaneously form a lateral offset, ΔL, from said source region and said drain region to the sidewalls of said gate electrode; and

forming a data line in electrical contact with said source region and crossing over said gate line at a cross-over location, wherein said overlying gate insulator is located between said data line and said gate line at said cross-over location to insulate said data line from said gate line.

24. The method of claim 23 wherein said gate electrode is comprised of tantalum, and wherein said overlying gate insulator comprises tantalum oxide.

25. The method of claim 23 wherein said gate electrode is selected from the group consisting of tantalum and aluminum.

26. The method of claim 23 wherein the semiconductor layer is a silicon layer formed by decomposing a silane gas using CVD.

27. The method of claim 23 wherein the semiconductor layer is a polysilicon layer formed by first forming an amorphous silicon layer and annealing the amorphous silicon layer at a temperature within a range of 450° C. to 700° C. for 12 to 70 hours.

28. The method of claim 23 wherein the gate insulating film is sputter formed on a surface of the semiconductor layer.

29. The method of claim 23 wherein the source region and the drain region are formed by implanting phosphorous ions into the semiconductor layer through the gate insulating film.

30. The method of claim 29 wherein the implanted phosphorous ions are radiated with a laser to reduce the resistance level in the semiconductor layer.

31. The method as defined in claim 23 wherein the overlying gate insulator is formed having a lateral thickness, ΔI, which is greater than the lateral offset, ΔL.

32. The method as defined in claim 23 wherein the step of forming the overlying gate insulator by anodic oxidation decreases the width of the gate electrode by about twice the lateral offset, ΔL.--

REMARKS

As discussed hereinafter, new claims 23-32 have been added to initiate an interference with U.S. Patent No. 5,561,075 ('075), the '075 patent being based on a Rule 60 divisional application of U.S. Patent No. 5,383,366 to Nakazawa wherein the claims of the '366 patent are device claims and those of the '075 patent are method claims.

The attention of the Examiner is directed to the filing of an Amendment under 37 CFR 1.607 in Serial No. 08/504,225, the '225 application being the parent of the present Rule 60 divisional application. In particular, the purpose of the foregoing Amendment under 37 CFR 1.607 is to initiate an interference with respect to the device claims of the above-mentioned '366 patent.

Moreover, an Amendment under 37 CFR 1.607 has also been filed in application Serial No. 08/223,823 to also initiate an interference with the foregoing '366 patent. In fact, the claims added to the '225 application are exactly the same as those added to the '823 application. In this regard the issue fee was paid in the '823 application on April 7, 1997, and thus a Petition under 37 CFR 1.313(b)(4) has also been filed to withdraw the '823 application from issue.

Furthermore, upon grant of the foregoing Rule 313(b)(4) Petition and declarations of interferences in the '225 and '823 applications, it has been requested that the foregoing interferences be consolidated into a single interference in view of the fact that the claims added to the '225 and '823 applications are exactly the same.

New claims 23-32 in this Rule 60 divisional application are substantially copied from U.S. Patent No. 5,561,075 to Nakazawa (hereinafter Nakazawa '075 or the '075 patent), a copy of which is submitted herewith. Claims 23-24 and 29-32 are exactly the same as claims 1-2, and 9-12 of the '075 patent and claims 25-28 are generally related to claims 3 and 6-8 of the '075 patent. In accordance with 37 CFR §1.607(a)(5), copied claims 23-32 may be applied to applicant's disclosure as shown in the claims analysis attached thereto as Exhibit A.

In accordance with 37 CFR §1.607(a)(2), applicant presents the following proposed count 1, wherein claim 1 of the '075 patent and claim 23 submitted herewith each correspond exactly to count 1:

1. A method of manufacturing an active matrix panel in which data signals are supplied to liquid crystal layers through a plurality of thin film transistors arranged in a matrix of pixels, gate lines and data lines being coupled to each thin film transistor, said method comprising the steps of:

forming a semiconductor layer on a substrate;

forming a gate insulating film on said semiconductor layer;

forming a gate electrode above said gate insulating film and a gate line in electrical contact with said gate electrode;

forming a source region and a drain region in said semiconductor layer by adding impurities thereto as donors or acceptors using said gate electrode as a self alignment mask;

simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line and simultaneously form a lateral offset, ΔL, from said source region and said drain region to the sidewalls of said gate electrode; and

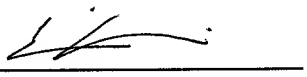
forming a data line in electrical contact with said source region and crossing over said gate line at a cross-over location, wherein said overlying gate insulator is located between said data line and said gate line at said cross-over location to insulate said data line from said gate line.

With respect to the foregoing, the attention of the Examiner is directed to the fact that, during the prosecution of application Serial No. 07/880,120 (a predecessor application upon which the '075 patent is based), the party Nakazawa filed a verified English translation of one of their Japanese priority applications on July 13, 1994 in order to avoid a rejection under 35 U.S.C. § 102 based on U.S. Patent Number 5,289,030, which patent

issued on a predecessor application of the subject application. In particular, the party Nakazawa attempted to obtain a Japanese filing date earlier than the effective U.S. filing date of the subject application. However, as demonstrated herein and below, the present applicant is entitled to an earlier Japanese filing date than the earliest Japanese filing date of the party Nakazawa with respect to at least claims 23, 25-29, and 31-32.

Verified English translations of the Japanese priority applications (Nos. 3-65418 filed March 6, 1991 and 3-135569 filed May 11, 1991) for the present application are submitted herewith. Newly presented claims 23-32 can be read on these priority applications as shown in Exhibit B. As can be seen, applicant is entitled to the March 6, 1991 priority date for at least claims 23, 25-29 and 31-32. Since applicant's March 6, 1991 priority date is earlier than the May 8, 1991 priority date of the '366 patent, applicant respectfully requests that it be designated senior priority in a declaration of the interference.

Respectfully submitted,



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PENDING CLAIMS	SUPPORT IN JAPANESE PRIORITY APPLICATION 3-65418 (FILED MARCH 6, 1991) OR JAPANESE PRIORITY APPLICATION 3-135569 (FILED MAY 11, 1991)
23. A method of manufacturing an active matrix panel in which data signals are supplied to liquid crystal layers through a plurality of thin film transistors arranged in a matrix of pixels, gate lines and data lines being coupled to each thin film transistor, said method comprising the steps of:	(JP 3-65418); Paragraphs [0022] and [0023]; Figure 4 Figure 4 shows an active matrix liquid crystal display circuit. Data signals are supplied to liquid crystal layers through a plurality of thin film transistors 21, 22 arranged in a matrix of pixels. Gate lines and data lines (such as gate line 50 and data lines 52 and 53) are connected to each transistor.
forming a semiconductor layer on a substrate;	(JP 3-65418); Paragraph [0026]; Figure 3A A semiconductor (silicon) layer is formed on substrate 1.
forming a gate insulating film on said semiconductor layer;	(JP 3-65418); Paragraph [0040]; Figure 3B A gate insulating film 27 is formed on the semiconductor (silicon) layer as shown in Figure 3B.
forming a gate electrode above said gate insulating film and a gate line in electrical contact with said gate electrode;	(JP 3-65418); Paragraphs [0018] and [0041]; Figures 3B and 4 Gate electrode 25 is formed above gate insulating film 27 (Figure 3B) and gate line 50 is formed in electrical contact with gate electrode 25 (Figure 4).
forming a source region and a drain region in said semiconductor layer by adding impurities thereto as donors or acceptors using said gate electrode as a self alignment mask;	(JP 3-65418); Paragraphs [0039], [0042]-[0043], [0047], and [0065]; Figures 3D Source region 35 and drain region 33 are formed in the semiconductor (silicon) layer by adding either boron (acceptor) or phosphorous (donor) impurities, using the gate electrode as a self-alignment mask as discussed in paragraphs [0047] and [0065].
simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line and simultaneously form a lateral offset, ΔL, from said source region and said drain region to the sidewalls of said gate electrode; and	(JP 3-65418); Paragraphs [0016], [0018], [0042]-[0043], [0050]; Figures 1, 3E and 3G As clearly illustrated in Figure 1 source and drain regions 3 are laterally offset by a distance L from each of the adjacent sidewalls of the gate electrode 8, which is covered with aluminum oxide 10. Similarly, in Figure 3G, source region 35 and drain region 33 both have a lateral offset from the side edges of gate electrode 25, which is covered by aluminum oxide layer 40 formed by anodic oxidation. As is further discussed with respect to the following clause of this claim, paragraph [0018] states that the same anodic oxide film covers both the gate electrode and gate wiring. Therefore, the anodic oxide film formed on the gate electrode and the gate line is formed at the same time. The anodic oxidation process necessarily must reduce the dimensions of the gate electrode as stated, for example, in column 3, lines 44-55 of U.S. Patent 5,583,366.

PENDING CLAIMS	SUPPORT IN JAPANESE PRIORITY APPLICATION 3-65418 (FILED MARCH 6, 1991) OR JAPANESE PRIORITY APPLICATION 3-135569 (FILED MAY 11, 1991)
forming a data line in electrical contact with said source region and crossing over said gate line at a cross-over location, wherein said overlying gate insulator is located between said data line and said gate line at said cross-over location to insulate said data line from said gate line.	(JP 3-65418); Paragraphs [0018], [0041], and [0052]; Figures 3B and 3G Data line 53 is coupled to thin film transistor 22, and crosses over gate line 50 at a cross-over location, as shown in Figure 4. Paragraph [0018] of the specification supports this limitation by disclosing that "stereoscopic wirings can be easily made on this aluminum oxide film by crossing wirings of another wiring such as the source electrode . . . ." (Emphasis added). Thus, the aluminum oxide film formed on the gate electrode is the same aluminum oxide film that insulates the gate electrode 50 from the source line 53, which crosses over the aluminum oxide. Since the aluminum oxide film is formed both on the gate electrodes 25, 26 and gate line 50, paragraph [0018] clearly discloses that another wiring, such as the source electrode wiring 53, crosses the gate line at a cross-over location. Also see paragraph [0063] in this regard.
24. The method of claim 23 wherein said gate electrode is comprised of tantalum, and wherein said overlying gate insulator comprises tantalum oxide.	(JP 3-135569); Paragraphs [0037] and [0040] Paragraph [0037] discloses that the gate electrode could be comprised of tantalum. Paragraph [0040] discloses that anodic oxidation of the gate electrode is performed, which would necessarily result in tantalum oxide being formed.
25. The method of claim 23 wherein said gate electrode is selected from the group consisting of tantalum and aluminum.	(JP 3-65418); Paragraphs [0041] and [0050]; Figures 3B and 3E As disclosed in paragraph [0041], gate electrode 25 is formed from aluminum (Figure 3B). Aluminum oxide is formed around gate electrode 25 by anodic oxidation (paragraph [0050]). (JP 3-135569); Paragraphs [0037] and [0040] Paragraph [0037] discloses that the gate electrode could be comprised of tantalum. Paragraph [0040] discloses that anodic oxidation of the gate electrode is performed, which would necessarily result in tantalum oxide being formed.
26. The method of claim 23 wherein the semiconductor layer is a silicon layer formed by decomposing a silane gas using CVD.	(JP 3-65418); Paragraphs [0026]-[0028] The semiconductor layer is silicon formed by decomposing monosilane, disilane, or trisilane using either plasma CVD or low pressure CVD.

PENDING CLAIMS	SUPPORT IN JAPANESE PRIORITY APPLICATION 3-65418 (FILED MARCH 6, 1991) OR JAPANESE PRIORITY APPLICATION 3-135569 (FILED MAY 11, 1991)
27. The method of claim 23 wherein the semiconductor layer is a polysilicon layer formed by first forming an amorphous silicon layer and annealing the amorphous silicon layer at a temperature within a range of 450° C. to 700° C. for 12 to 70 hours.	(JP 3-65418); Paragraphs [0031]-[0033] As described in paragraph [0031], a deposited amorphous silicon film is heated at a temperature of 450-700 °C for 12-70 hours to increase the crystallinity of the film (paragraph [0033]).
28. The method of claim 23 wherein the gate insulating film is sputter formed on a surface of the semiconductor layer.	(JP 3-65418); Paragraphs [0026]-[0027]
29. The method of claim 23 wherein the source region and the drain region are formed by implanting phosphorous ions into the semiconductor layer through the gate insulating film.	(JP 3-65418); Paragraphs [0043]-[0044] Source 35 and drain 33 are formed from implanting phosphorous through gate insulating film 27 as described in paragraphs [0043]-[0044].
30. The method of claim 29 wherein the implanted phosphorous ions are radiated with a laser to reduce the resistance level in the semiconductor layer.	(JP 3-135569); Paragraphs [0022] and [0044] Paragraphs [0022] and [0044] both disclose laser irradiation of source/drain regions including phosphorous to activate these regions and thus reduce the resistance level in the semiconductor layer.
31. The method as defined in claim 23 wherein the overlying gate insulator is formed having a lateral thickness, ΔI, which is greater than the lateral offset, ΔL.	(JP 3-65418); Paragraphs [0016], [0042]-[0043], [0050]; Figures 1, 3E and 3G During the process described with respect to the formation of the device, source region 35 and drain region 33 are formed (paragraphs [0042]-[0043]) before anodic oxide coating 40 is formed (paragraph [0050]). The process described must necessarily result in a thickness of the oxide layer being greater than the lateral offset distance L between source and drain regions and the adjacent edge of the gate electrode. That is, since the source and drain regions are formed using the gate electrode as a mask, and the gate electrode is subsequently anodically oxidized, the thickness of the oxide layer will inherently be greater than the lateral offset distance L.

PENDING CLAIMS	SUPPORT IN JAPANESE PRIORITY APPLICATION 3-65418 (FILED MARCH 6, 1991) OR JAPANESE PRIORITY APPLICATION 3-135569 (FILED MAY 11, 1991)
32. The method as defined in claim 23 wherein the step of forming the overlying gate insulator by anodic oxidation decreases the width of the gate electrode by about twice the lateral offset, ΔL.	The claimed reduction in width of the gate electrode is an inherent result of the described process. That is, source and drain regions are formed using the gate electrode as a mask, and the gate electrode is subsequently anodically oxidized and reduced in width as discussed in connection with claim 1 above. Since the lateral offset is defined to be the distance from the source region and the drain region to the sidewalls of the gate electrode, and this distance is equal to the amount of reduction in the size of the gate electrode on either side, the gate electrode will necessarily be reduced by about twice the lateral offset, ΔL.

TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device and a method for forming the same. More particularly, the present invention relates to a thin film transistor applicable to liquid crystal electro-optical devices, contact type image sensors, and the like.

2. Description of the Prior Art

Insulated gate field effect semiconductor devices known to the present have been widely applied to various fields. Such semiconductor devices comprise a silicon substrate having integrated thereon a plurality of semiconductor elements so that the devices may function as integrated circuits (ICs) and large scale integrated circuits (LSIs).

In addition to the insulated gate field effect semiconductor devices of the type mentioned above, there is another type of such insulated gate field effect semiconductor devices which comprises a thin film semiconductor formed on an insulator substrate, rather than a silicon substrate. Those thin film insulated gate field effect semiconductor devices (referred to hereinafter as TFTs) are now more positively used, for example, in liquid crystal electro-optical devices as switching elements of pixels and driver circuits, and in read-out circuits of contact type image sensors and the like.

Those TFTs are produced, as mentioned above, by laminating thin films on an insulator substrate by a vapor phase process. This process can be conducted in an atmosphere controlled to a temperature as low as about 500°C, or even lower. Moreover, low

cost substrates such those made of soda-lime glass and borosilicate glass can be utilized in those TFTs. Thus, the insulated gate field effect semiconductor device of the latter type are advantageous in that they can be fabricated using low cost substrates, and that they can be readily scaled up by depositing the thin films on a substrate having a larger area with the only limiting factor being the dimension of the apparatus in which the thin films are vapor-phase deposited. Accordingly, application of such insulated gate field effect semiconductor devices to liquid crystal electro-optical devices having a large pixel matrix structure or to a one- or two-dimensional image sensors has been expected, and, in fact, a part of such expectations has been met already.

A representative structure for the latter type of TFTs is shown schematically in FIGS. 2 and 6.

Referring to FIG. 2, a typical structure of a conventionally known TFT is explained. In FIG. 2, a thin film semiconductor 2 made of an amorphous semiconductor is deposited on a glass insulator substrate 1, and the thin film 2 comprises on the surface thereof a source area and a drain area 3, source and drain contacts 7, and a gate 11.

Those types of TFTs comprise, as mentioned above, semiconductor layers having deposited by a vapor deposition process. Since the electron and hole mobilities of the semiconductor layers in those TFTs are significantly low as compared with those of the conventional ICs and LSIs, it has been customary to subject the semiconductor layer 2 to a heat treatment for the crystallization thereof.

In a conventional TFT as shown in FIG. 2, the gate 11 is covered with a relatively thick interlayer insulator film 4 such as a silicon nitride film and a silicon oxide film, and to this interlayer insulator film are provided contact holes by a

photolithographic process. The source and drain contacts 7 are electrically connected with source and drain areas 3. If feeding points to the source and the drain were to be provided at such positions, the distance L between each of the feeding points and the channel end becomes considerably long.

As mentioned earlier, the TFTs fabricated by a thin film deposition process at low temperatures are significantly low in the carrier mobility. Even upon doping an impurity, the still low conductivity produces a resistance within this distance L. Accordingly, the conventional TFTs suffer poor frequency characteristics and increase in ON circuit resistance. Furthermore, the area necessary for a TFT increases inevitably with increasing length of L. This made it difficult to accommodate a predetermined number of TFTs within a substrate of a limited dimension.

In FIG. 6, a thin film semiconductor 102 composed of an amorphous semiconductor is deposited on a glass insulator substrate 101, and the thin film 102 comprises on the surface thereof a source and a drain area 103, source and drain electrodes 107, and a gate 111.

The TFTs of this type in general are produced by first depositing a semiconductor film on the substrate, and, by patterning, forming island-like semiconductor areas 102 on the desired parts using a first mask. Then, an insulating film and further thereon a gate material are formed, from which a gate electrode 111 and a gate insulating film 106 are obtained by patterning using a second mask. A source and a drain area 103 are established on the semiconductor areas 102 in a self-aligned manner, using the gate electrode 111 and a photoresist formed using a third mask as masks. An interlayer insulator film 104 is formed thereafter. To this interlayer insulator film are provided contact holes using a fourth mask, so that the contacts

may be connected to the source and the drain through those contact holes. A contact material is provided to the resulting structure thereafter, which is patterned to form contacts 107 using a fifth mask. Thus is obtained a complete TFT.

As can be seen from the foregoing description, a TFT in general requires five masks to complete a structure, and in a complementary TFT, six masks are necessary. Naturally, a more complicated IC should incorporate further more masks. The use of increased number of masks involves a complicated process for fabricating a TFT element, which accompanies frequent mask alignment steps. Such a complicated process inevitably results in a lowered yield and productivity of the TFT elements. The demand for larger electronic devices using the TFT elements, for making the TFT elements themselves more compact, and for finer patterning, makes the yield and productivity even worse. Thus, it has been desired to develop a simpler process which involves no complicated steps, and a TFT based on a novel structure which requires less masks.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a semiconductor device based on a novel structure.

Another object of the present invention is to provide an insulated gate field effect semiconductor device having each of the feeding points for source and drain in proximity to the channel region at a shorter distance to the channel ends.

Still another object of the present invention is to provide a method for forming semiconductor devices using less masks.

The insulated gate field effect semiconductor device according to the present invention is characterized by that the TFT comprises a metal gate electrode having at least to the side thereof a film of an anodically oxidized gate electrode material.

The insulated gate field effect semiconductor device according to the present invention is also characterized by that the contact hole for the extracting contacts of the source and drain semiconductor regions are provided at about the same position of the end face of the anodically oxidized film established at the side of the gate electrode.

To improve the carrier mobility in the semiconductor layer of the insulated gate field effect semiconductor device according to the present invention, if necessary, the substrate having deposited thereon a silicon semiconductor film containing hydrogen therein may be subjected to thermal treatment to thereby modify said semiconductor film into such having a crystalline structure. Furthermore, to minimize the distance L between the feeding points and the channel ends, a metal gate electrode may be provided, e.g., an aluminum gate electrode, and the outer (peripheral portion) of this gate electrode may be oxidized then to form at least on the side thereof a metal oxide film, e.g., an aluminum oxide film.

Furthermore, the gate electrode together with the aluminum oxide film surrounding said gate electrode may be used as a mask to form contact holes for the extract contacts of the source and the drain with a side surface of the contact hole located substantially on a side surface of the aluminum oxide film in a self-aligned manner. The present invention provides, as is shown in the schematic cross sectional view of FIG. 1, a TFT comprising a metal gate electrode 8 having at least on the side thereof an oxide layer 10 comprising the metal, e.g. an aluminum oxide layer, to which source and drain electrodes 7 (contacts for a drain and a source) connected to the source and drain semiconductor regions respectively are provided approximately at the end of the oxide layer. The source and drain electrodes 7 are connected to the source and drain semiconductor regions 3. By

taking such a construction, a shorter distance L between said feeding points and the channels has been achieved. In Fig.1, a channel is located adjacent to the gate electrode 8 between the source and drain semiconductor regions 3 under a gate insulating film 6. In Fig.1, the gate insulating film 6 is provided between the channel and the gate electrode 8. In Fig.1, a side of at least one of the source and drain electrodes 7 is substantially aligned with a side of the oxide layer 10. In Fig.1, the oxide layer is in contact with the gate electrode and at least one of the source and drain electrodes. In Fig.1, a side of the source semiconductor region is aligned with a side of the oxide layer and also a side of the drain semiconductor region is aligned with a side of the oxide layer.

Ideally, it is favorable to reduce the distance L to zero from the viewpoint of lowering the resistance (in FIG. 1, indeed, the distance L is approximately zero). However, difficulties ascribed to process technology, for example, a small extension of the source and the drain semiconductor regions under the gate, hinder achievement of a complete zero. Nevertheless, a shorter distance L still promises a considerable effect in reducing the resistance.

In the embodiment exemplified by FIG. 1, the aluminum oxide film around the gate electrode is established over the side and the upper plane of the gate electrode, i.e., over the whole outer plane exposed to the outside. However, the aluminum oxide film according to the present invention not necessarily be provided to the whole outer surrounding. The aluminum oxide film should be provided at least to cover the side of the gate electrode to shorten the distance L. If the aluminum oxide film is provided to the whole outer as is shown in FIG. 1, this film can be used as it is as a part of a mask at the fabrication of the contact holes, because the aluminum oxide film is hardly etched.

Furthermore, other wiring, e.g., a wiring for the source electrode, may be crossed over this aluminum oxide film to establish a three-dimensional wiring which facilitates the later process steps for integration.

In the insulated gate field effect semiconductor device according to the present invention, what is meant by providing the contact holes for the extract contacts of the source and the drain in an approximately the same position as that of the ends of the gate electrode and the aluminum oxide film, is a structure resulting upon formation of contact holes in a self-aligned manner using the ends of the gate electrode and the aluminum oxide film, as well as a structure having a slight positional deviation in the case of using masks at the positioning, ascribed to the incomplete alignment of the masks. Referring to FIG. 1, for example, the edge portion of the insulator film 9 is sometimes displaced from the end of the aluminum oxide at the mask alignment when the contact portion alone is intended to form. Such a case is included in the latter case mentioned hereinbefore. In the former case taking advantage of the aluminum oxide film as a mask, i.e., in the case of extending the etching area of the insulator film up to the gate, the insulator film 9 can be completely removed from the gate, and the end of the source or the drain is certainly aligned with that of the aluminum oxide film 10 to result in a shortened distance L.

The aluminum oxide may be provided around the gate electrode by anodically oxidizing said gate electrode. The anodic oxidation process comprises applying an electric current to a metal gate electrode having dipped in an acidic solution to oxidize the surface thereof by an electrochemical reaction. There may be used other processes, provided that the oxide film has a dense structure and that the oxidation can be effected rapidly.

The insulated gate field effect semiconductor device

according to the present invention is also characterized by that it comprises a TFT gate electrode surrounded by an anodically oxidized film of the same material constituting the gate electrode, with the contacts (source and drain electrodes) connected to the source and the drain being brought into contact with the upper planes and the sides of the source and the drain each, and that said contacts (source and drain electrodes) being connected to each of the drain and the source extend on the upper surface of the oxidized film having provided surrounding said gate electrode.

As shown in the schematically shown cross sectional view of FIG. 5, the TFT according to the present invention comprises an anodically oxidized film 110 at least as the surroundings of the gate electrode 108 comprising a metal, with the upper planes and the sides of the source and drain semiconductor regions slightly sticking out from the ends of said anodically oxidized film. The source and drain semiconductor regions are connected to the contacts 107 (source and drain electrodes) through these slightly sticking out portions (that is, the upper planes and the sides of the source and drain semiconductor regions) to make the area of connection larger. Furthermore, the contacts 107 are extended over the upper portion of the anodically oxidized film 110, at which they are patterned into separate electrodes. In Fig.5, a channel is located adjacent to the gate electrode 108 between the source and drain semiconductor regions 103 under a gate insulating film 106. In Fig.5, the gate insulating film 106 is provided between the channel and the gate electrode 108. In Fig.5, said anodically oxidized film 110 is provided between the gate electrode 108 and the source and drain electrodes 107.

Referring to FIG. 7, a fabrication process for the TFT according to an embodiment of the present invention and having the structure illustrated in FIG. 5 is explained. The FIG. 7 is

provided as an explanatory means and the details concerning dimension and shape are a little different from those of the actual device.

First, as in FIG. 7 (A), on a glass substrate, e. g., a substrate of a heat-resistant crystallized glass 101, is deposited a semiconductor layer 102. The semiconductor layer, e. g., a silicon semiconductor layer, may be an amorphous semiconductor, a polycrystalline semiconductor, or any other selected from a wide variation, and may be deposited by processes such as a plasma-assisted CVD (chemical vapor deposition), sputtering, and pyrolytic CVD, depending on the type of the semiconductor used. In the following explanation, the process steps are described according to a case in which a polycrystalline silicon semiconductor is used. The next step in the fabrication process comprises forming a silicon oxide film 106 on the semiconductor layer 102, so that the silicon oxide film 106 may function as the gate insulating film. Further on the silicon oxide film is formed an contact material layer, an aluminum layer in this case, from which a gate electrode is established. The contact material layer is then patterned into the gate electrode 108 using a first mask (21). An anodically oxidized film is provided as a surrounding of the gate electrode 108, by conducting an anodic oxidation in an electrolyte for the anodic oxidation. A pore-free aluminum oxide 110 can be provided at least at the vicinity of the channel region to the surrounding of the gate electrode, as illustrated in FIG.7 (B).

The electrolyte to be used in the anodic oxidation includes, representatively, strong acid solutions of, such as sulfuric acid, nitric acid, and phosphoric acid, as well as mixed acid comprising tartaric acid or citric acid, having added therein ethylene glycol or propylene glycol or the like. The solution (electrolyte) may be further mixed with a salt or an alkaline

solution to adjust the solution (electrolyte) for the pH value.

The anodic oxidation was performed as follows. The substrate was immersed into an AGW electrolyte having prepared by adding 9 parts of propylene glycol to 1 part of an aqueous 3% tartaric acid solution. A direct current (D.C.) was applied to the substrate by connecting the aluminum gate to the anode of a power source and using a platinum cathode as the counter electrode. The electric current was applied first at a constant current density of 3 mA/cm^2 for 20 minutes, and then at a constant voltage for 5 minutes, to thereby obtain a 1,500 Å thick aluminum oxide film around the gate electrode. The insulating properties of this aluminum oxide film was evaluated using a specimen having subjected to an oxidation treatment under the same condition as that employed above. As a result, a resistivity of 10^{15} Ω and a dielectric breakdown of 3×10^6 V/cm was obtained for the film. The surface of the sample was observed through a scanning electron microscope to find surface irregularities at a magnification of about 10,000, but no minute holes. The film was therefore evaluated as a favorable insulator coating.

On the surface of the thus obtained insulator film was further deposited a silicon oxide film 112 by plasma-assisted CVD. The film was then anisotropically etched along a direction nearly vertical to the substrate to leave over silicon oxide 113 on the side walls of the protrusion constructed by the gate electrode and the anodically oxidized film (see FIG. 7(D)). The semiconductor layer 102 is then removed by etching in a self-aligned manner using the remaining silicon oxide film 113, and the gate electrode 108 and the anodically oxidized film 110 of the protrusion as a mask. The resulting structure is shown in FIG. 7(E). The structure as viewed from the upper side is shown in FIG. 8(A). The cross sectional view taken along the line A-A' indicated in FIG. 8(A) is given in FIG. 7.

The structure as shown in FIG. 7(E) was subjected to a selective etching to remove only silicon oxide, i.e., the silicon oxide film 113 and the gate insulating film, using the gate electrode 108 and the anodically oxidized film 110 thereof as the mask, to thereby obtain a structure having a part of the semiconductor layer 102 exposed to outside at the edge of the gate, as shown in FIG. 7(F) and FIG. 8(B).

The resulting semiconductor portion exposed to the air is then doped with impurities to establish a source and a drain. As can be seen in FIG. 7(F), the part exposed to the air was bombarded with phosphorus ions from the upper side of the substrate using the anodically oxidized film 110 of the gate electrode as the mask. Thus are formed the source and drain regions 103. In Fig.7(F), sides of the source and drain regions 103 are located at sides of the semiconductor portion exposed to the air. For the activation of the regions, a laser beam is irradiated to the exposed portions. Instead of carrying out the laser annealing as the activation treatment of the source and the drain regions, they can be otherwise activated by thermal annealing and the like.

An aluminum layer is then formed on the upper surface of the resulting structure, which is separated into source and drain electrodes by etching the aluminum layer into a predetermined pattern using a second mask (22). The structure obtained in this step is shown in FIG. 8(C). This structure is then finished into a TFT shown in FIGS. 7(G) and 8(D), by removing the unnecessary portions of the semiconductor layer 102 using the source and the drain electrodes 107 and the anodically oxidized film 110 on the gate electrode as the mask.

It can be seen from the foregoing description that the present invention provides a TFT by involving merely 2 masks.

In the case of a complementary TFT, 1 or 2 more masks

suffice the fabrication of the structure.

The TFT thus obtained can be connected to the outer through a non-oxidized part of the gate electrode left out at the anodic oxidation, by carrying out the anodic oxidation treatment with care not to contact the part of the gate electrode with the electrolyte used at the anodic oxidation, or through a non-oxidized part of the gate electrode produced by selectively etching the anodically oxidized film exposed to the outer at the final step of selective etching of the source and drain electrodes together with the accompanying anodically oxidized film, after etching the unnecessary semiconductor layer. Otherwise, a contact hole may be perforated in a specific anodically oxidized film, using a third mask.

The foregoing description for the fabrication of a TFT is merely an example, and it should be understood that the present invention is not limited thereto. For example, the source and the drain regions may be doped with impurities by ion-bombardment at the stage shown in FIG. 7(B) using the anodically oxidized film 110 of the gate electrode as the mask, instead of carrying out the doping step after the patterning of the semiconductor layer 102 as demonstrated above in FIG. 7(F).

Furthermore, after the semiconductor layer 102 is established and before forming a gate, another photomask can be incorporated to carry out patterning of the semiconductor layer at the proximity of the TFT area into an island-like structure. Thus can be obtained a structure as shown in FIG. 9, which comprises only the substrate or an insulator film established on the substrate under the lead wiring instead of the semiconductor layer 102. Such a configuration avoids establishment of a capacitor which may otherwise be formed by the gate wiring and a semiconductor layer. In this manner can a TFT of an increased response be fabricated by using only 3 masks. The structure as

viewed from the upper side is given in FIG. 9(A), and the cross sectional view along the line B-B' is given in FIG. 9(B).

In a general structure for an insulated gate field effect semiconductor device according to the present invention as shown in FIG. 5, the end of the gate is displaced from the position of the end of the source or the drain region by the thickness of the insulator film (anodically oxidized film) provided around the gate. Such an offset structure decreases the carrier density at the channel and, at the same time, reduces the electric field intensity at the drain-channel junction that the drain breakdown voltage can be improved. Since the thickness of the insulator film may be varied in the range of, for example, from 10 to 50 nm by changing the condition at the oxidation, the amount of this offset can be readily set as desired, depending on the required device characteristics. Furthermore, a lightly doped drain (LDD) structure can be realized by controlling the impurity concentration of this offset portion to a value lower than that in the source and the drain regions.

In Fig.5, a channel length (a distance between the source and the drain regions) is longer than a length of the gate electrode in a direction of the channel length.

An offset region to which no electric field or very weak electric field is applied by a gate voltage can be formed in a portion of a channel region in contact with a source or a drain region in an insulated gate field effect transistor in which a channel length thereof is longer than a length of a gate electrode thereof in a direction of the channel length. For example, in Fig.5, no electric field is applied to the offset region located in the channel region in the semiconductor 102 between a portion of the channel region just under the gate electrode 108 and the source or the drain region, a very weak electric field is applied to the offset region as compared with

an electric field applied to the portion of the channel region just under the gate electrode 108. In Fig.5, for example, the channel length is longer than the length of the gate electrode 108 in the direction of the channel length by an approximately twofold thickness of the insulator film (anodically oxidized film).

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 shows a schematically drawn cross sectional view of an insulated gate field effect semiconductor device according to an embodiment of the present invention;

FIG.2 shows a schematically drawn cross sectional view of a conventional insulated gate field effect semiconductor device;

FIG.3 shows a fabrication process of an insulated gate field effect semiconductor device according to an embodiment of the present invention;

FIG. 4 shows a circuit diagram of a liquid crystal electro-optical device to which an insulated gate field effect semiconductor device according to an embodiment of the present invention is applied;

FIG. 5 shows the structure of a TFT according to an embodiment of the present invention;

FIG. 6 shows the structure of a conventional TFT;

FIG. 7 shows a schematically shown cross sectional view of a TFT according to the present invention to illustrate the fabrication step thereof;

FIG. 8 shows a schematically shown view seen from the upper side of a TFT according to the present invention to illustrate the fabrication step thereof;

FIG. 9 shows the structure of another TFT according to the present invention;

FIG. 10 shows a schematically drawn circuit diagram of a

liquid crystal electro-optical device to which a complementary TFT according to an embodiment of the present invention is applied;

FIG. 11 shows a schematically drawn cross-sectional view illustrating a fabrication process of a liquid crystal electro-optical device to which a complementary TFT according to an embodiment of the present invention is applied;

FIG. 12 shows a schematically drawn diagram indicating the mounted arrangement on the substrate of a liquid crystal electro-optical device to which a complementary TFT according to an embodiment of the present invention is applied;

FIG. 13 shows a schematically drawn circuit diagram of a liquid crystal electro-optical device to which a complementary TFT according to another embodiment of the present invention is applied; and

FIG. 14 shows a schematically drawn diagram indicating the mounted arrangement on the substrate of a liquid crystal electro-optical device to which a complementary TFT according to another embodiment of the present invention is applied.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Now the present invention is described in further detail below referring to some EXAMPLES, however, it should be noted that the present invention is not to be construed as being limited thereto.

EXAMPLE 1

Referring to FIG. 4, an example in which a TFT according to the present invention is applied to a liquid crystal electro-optical device having a diagram as illustrated i Fig.4 is described. In FIG. 4, an N-channel TFT (N-TFT) 22 and a P-channel TFT (P-TFT) 21 in a complementary configuration are provided to

each of the pixels of the liquid crystal device. Each of the TFTs are connected to a common signal wire 50 through respective gate electrodes, and the output terminals of the N-TFT 22 and the P-TFT 21 are connected to the common pixel electrode 43, whereas each of the other output terminals 28 and 35 in the respective TFTs is connected to the other signal wires 52 and 53 to provide an inverter structure. The positions of the P-TFT and the N-TFT may be reversed to establish a buffer structure and provide the complementary TFTs to each of the pixel electrodes.

Referring to FIGS. 3(A) to 3(G), the fabrication process of a complementary TFT (C/TFT) on a substrate according to the present invention to be used in a liquid crystal electro-optical device is described below.

In FIG. 3(A), a silicon oxide film from 1000 to 3000 Å in thickness as a blocking layer 24 was deposited by radio-frequency (RF) magnetron sputtering on a non-expensive glass substrate 1 which is resistant to a heat treatment at a temperature of 700°C or lower, e.g. about 600°C. Examples of such glasses useful as the substrate include crystallized glass such as AN glass and neo-ceramic glass, and Vycor® 7913 (a heat resistant glass manufactured by Corning Corp.).

The silicon oxide film was deposited in a 100% oxygen atmosphere at the deposition temperature of 150°C, at an output of from 400 to 800 W and a pressure of 0.5 Pa. The target used was quartz or single crystal silicon, and thus was obtained the film at a film deposition rate of from 30 to 100 Å/minute.

An amorphous silicon film was deposited on the silicon oxide blocking layer by any of the processes of low pressure chemical vapor deposition (LPCVD), sputtering, and plasma-assisted CVD (PCVD).

In the LPCVD process, film deposition was conducted at a temperature lower than the crystallization temperature by 100 to

200°C, i.e., in the range of from 450 to 550°C, e.g., at 530°C, by supplying disilane (Si_2H_6) or trisilane (Si_3H_8) to the CVD apparatus. The pressure inside the reaction chamber was controlled to be maintained in the range of from 30 to 300 Pa. The film deposition rate was 50 to 250 Å/minute. Furthermore, optionally boron may be supplied as diborane during the film deposition to control the threshold voltage (V_{th}) of the N-TFT to be approximately the same as that of the P-TFT.

The film deposition process by sputtering was conducted using a single crystal silicon as the target in an argon atmosphere having added therein from 20 to 80% of hydrogen, e.g., in a mixed gas atmosphere containing 20% of argon and 80% of hydrogen. The back pressure prior to sputtering was controlled to 1×10^{-5} Pa or lower. The film was deposited at a film deposition temperature of 150°C, a frequency of 13.56 MHz, a sputter output of from 400 to 800 W, and a pressure of 0.5 Pa.

In the deposition of a silicon film by a PCVD process, the temperature was maintained, e.g., at 300°C, and monosilane (SiH_4) or disilane (Si_2H_6) was used as the reacting gas. A high frequency electric power was applied at 13.56 MHz to the gas inside the PCVD apparatus to effect the film deposition.

The films thus obtained by any of the foregoing processes preferably contains oxygen at a concentration of 5×10^{21} cm^{-3} or lower, and more preferably, 7×10^{20} cm^{-3} or lower. If the oxygen concentration is too high, the film thus obtained would not crystallize. Accordingly, there would be required to elevate the thermal annealing temperature or to take a longer time for the thermal annealing. Too low an oxygen concentration, on the other hand, increases an off-state leak current due to a backlighting when the semiconductor layer is irradiated with a light beam in a liquid crystal electro-optical device. Accordingly, the oxygen concentration was set in the range of from 4×10^{19} to 4×10^{21}

cm^{-3} to readily crystallize the semiconductor layer by thermal annealing at a moderate temperature (600°C or lower). The hydrogen concentration was 4 x 10^{20} cm^{-3}, which accounts for 1 % by atomic with respect to the silicon concentration of 4 x 10^{22} cm^{-3}.

Oxygen concentration was controlled to 7 x 10^{20} cm^{-3} or lower, preferably 7 x 10^{19} cm^{-3} or lower, and more preferably 1 x 10^{19} cm^{-3} or lower to enhance crystallization of the source and drain regions, while selectively adding oxygen, carbon, or nitrogen by ion-implantation to a part of the channel forming regions of the TFT which constitute the pixel, to such an amount to give a concentration in the range of from 5 x 10^{19} to 5 x 10^{21} cm^{-3}, preferably 5 x 10^{20} to 5 x 10^{21} cm^{-3} to reduce the sensitivity to light. In a TFT fabricated in this manner, particularly in the TFT which constitutes the peripheral circuits, the oxygen concentration was lowered while a higher carrier mobility was imparted. This facilitated high frequency operation while the leak current of the TFTs at the OFF state in the pixel peripheral switching elements is reduced.

Thus was deposited an amorphous silicon film at a thickness of from 500 to 5,000 Å, e.g., at a thickness of 1,500 Å. The amorphous silicon film was then heat-treated at a moderate temperature in the range of from 450 to 700°C for a duration of from 12 to 70 hours in a non-oxidizing atmosphere. More specifically, for example, the film was maintained at 600°C under a hydrogen or nitrogen atmosphere.

Since on the surface of the substrate was provided an amorphous silicon oxide layer under the silicon film, the whole structure could be uniformly annealed because there generated no nucleus present during the heat treatment. That is, the silicon film during deposition maintains an amorphous structure, and hydrogen is present only as a free atom.

Then, at the annealing step, the silicon film undergoes phase transition from the amorphous structure to a structure having a higher degree of ordering, and partly develops a crystalline portion. Particularly, the region which attained a relatively high degree of ordering at the film deposition of silicon tend to crystallize at this stage. However, the silicon bonding which combines the silicon atoms to each other attracts an atom in a region to another in another regions. This effect can be observed by a laser Raman spectroscopy as a peak which is shifted to a lower frequency side as compared with the peak at 522 cm^{-1} for a single crystal silicon. The apparent grain size can be calculated by the half width as 50 to 500 Å, i.e., a size corresponding to that of a microcrystal, but, in fact, the film has a semi-amorphous structure comprising a plurality of those highly crystalline regions yielding a cluster structure, and the clusters are anchored to each other by the bonding between the silicon atoms (clustering). Thus was obtained a film having a semi-amorphous structure.

The semi-amorphous film thus obtained was subjected to a measurement of the elemental distribution along the direction of the depth, using, for example, a secondary ion mass spectroscopy (SIMS). The minimum concentration for the dopants (impurities) was found (either at the surface or at an inner portion apart from the surface) 3.4 x 10^{19} cm^{-3} for oxygen and 4 x 10^{17} cm^{-3} for nitrogen. Hydrogen was found at a concentration of 4 x 10^{20} cm^{-3}, which accounts for 1 % by atomic with respect to silicon which is present at a concentration of 4 x 10^{22} cm^{-3}. The crystallization could be achieved, for example, by a thermal treatment at 600°C for a duration of 48 hours in the case of a 1000 Å thick film containing oxygen at a concentration of 3.5 x 10^{19} cm^{-3}. Upon increasing the oxygen concentration of the film to 3 x 10^{20} cm^{-3} and considering the film thickness, it was

possible to crystallize a film as thick as in the thickness range of from 0.3 to 0.5 μm by annealing at 600 °C. However, a film having the same oxygen concentration but reduced in thickness to 0.1μm required a heat treatment at a higher temperature of 650°C for the crystallization. In short, a thicker film and a lower impurity (e.g., oxygen) concentration favored the crystallization.

The semi-amorphous film thus obtained yields, as a result, a state in which substantially no grain boundary (referred to hereinafter as GB) exists. Since the carrier easily moves between the clusters through the anchored portions, a carrier mobility far higher than that of a polycrystalline silicon having a distinct GB can be realized. More specifically, a hole mobility, μh, in the range of from 10 to 200 $cm^2/V \cdot sec$ and an electron mobility, μe, in the range of from 15 to 300 $cm^2/V \cdot sec$, are achieved.

On the other hand, if a high temperature annealing in the temperature range of from 900 to 1200°C were to be applied in the place of a moderate temperature annealing as described hereinabove, impurities undergo a solid phase growth from the nuclei and segregate in the film. This results in the high concentration of oxygen, carbon, nitrogen, and other impurities at the GB which develops a barrier. Thus, despite the high mobility within a single crystal, the carrier is interfered at its transfer from a crystal to another by the barrier at the GB. In practice, it is quite difficult to attain a mobility higher than or equal to 10 $cm^2/V \cdot sec$ with a polycrystalline silicon at the present.

Thus, in the EXAMPLE according to the present invention, a semi-amorphous silicon semiconductor is utilized. Otherwise, a polycrystalline silicon semiconductor can be utilized, provided that a sufficiently high carrier mobility therein can be achieved

therein.

Referring to FIG. 3(A), a process for fabricating an area 21 (having a channel width of 20 μm) for a P-TFT and an area 22 for an N-TFT at the right and left hand side, respectively, of FIG. 3(A) is described. The silicon film was masked with a first photomask ①, and subjected to photo-etching to obtain the areas.

On the resulting structure was deposited a silicon oxide film as a gate insulating film 27 to a thickness of from 500 to 2,000 Å, e.g., to a thickness of 1,000 Å. The conditions for the film deposition were the same as those employed in depositing the silicon oxide film to give a blocking layer. Further, a small amount of a halogen such as fluorine may be added during the film deposition to fix sodium ions.

Further on the gate insulating film was deposited an aluminum film at a thickness of 0.3 μm, which was subjected to patterning using a second photomask ②. Then, a gate 26 for the P-TFT and another gate 25 for the N-TFT were fabricated. The channel length was, for example, 10 μm.

In FIG. 3(C), a photoresist 31 was formed using a photomask ③, and then boron was doped to a source 28 and a drain 30 for P-TFT at a dose of 1×10^{15} cm^{-2}, by ion implantation.

Similarly, a photoresist 32 was formed using a photomask ④, and then phosphorus was doped to a source 35 and a drain 33 for N-TFT at a dose of 1×10^{15} cm^{-2}, by ion implantation.

The doping was conducted through the gate insulating film 27. However, as is shown in FIG. 3(B), the silicon oxide on the silicon film may be removed using the gate electrodes 25 and 26 as the masks, and then boron and phosphorus may be directly doped into the silicon film by ion implantation.

After removing the photoresist 32, the structure was re-heated at 650°C for a duration of 10 to 50 hours for annealing. Thus the impurities in the source 28 and the drain 30 of the P-

TFT, as well as those in the source 35 and the drain 33 of the N-TFT were activated to give P^+ and N^+.

Furthermore, channel forming regions 34 and 29 were provided as a semi-amorphous semiconductor or a polycrystalline semiconductor under the gate electrodes 25 and 26.

As described in the foregoing, a C/TFT can be fabricated in a self-aligned manner without heating it to a temperature of 700°C or higher. This allows use of a non-expensive substrates and excluding use of the expensive quartz substrate and the like. The process is therefore suitable for manufacturing liquid crystal display devices having many pixels. The thermal annealing was conducted twice, as shown in FIGS. 3(A) and 3(D). However, the annealing corresponding to that of FIG. 3(A) may be omitted depending on the required device characteristics, and the thermal annealing may be integrated into one corresponding to that of FIG. 3(D) to speed up the process.

In the present EXAMPLE, aluminum was used for the gate. This was effective for reducing the interface state density of the gate insulating film and also the loss of carriers, because at the annealing step corresponding to FIG. 3(D), the aluminum functioned effectively for dissociating hydrogen molecules incorporated in the gate insulating film into hydrogen atoms.

In the step corresponding to FIG. 3(E), the gate electrodes 25 and 26 were anodically oxidized to cover the surfaces thereof with aluminum oxide. More specifically, the substrate was dipped into a 13.7 % sulfuric acid bath, and to the substrate was applied a current at a density of 1 mA/cm^2 using a carbon anode placed at a distance of 30 cm from the substrate. Thus was formed aluminum oxide film at a thickness of from 0.2 to 1 μm, for example, at a thickness of 0.5 μm.

The solution to be used in the anodic oxidation include, representatively, strong acid solutions of, such as sulfuric

acid, nitric acid, and phosphoric acid, as well as mixed acid comprising tartaric acid or citric acid, having added therein ethylene glycol or propylene glycol or the like. A salt or an alkaline solution may be further added to the solution to thereby adjust the pH value of the solution.

The anodic oxidation was performed as follows. The substrate was immersed into an AGW electrolyte having prepared by adding 9 parts of propylene glycol to 1 part of an aqueous 3% tartaric acid solution. A direct current (D.C.) was applied to the substrate by connecting the aluminum gate electrode to the anode of a power source and using a carbon cathode as the counter electrode.

The electric current was applied first at a constant current density of 1 mA/cm^2 for 20 minutes, and then at a constant voltage for 5 minutes, to thereby obtain a 5,000 Å thick aluminum oxide film around the gate electrode. The insulating properties of this aluminum oxide film was evaluated using a specimen having subjected to an oxidation treatment under the same condition as that employed above. As a result, a resistivity of 10^9 Ω·m and a dielectric breakdown of 2×10^5 V/cm was obtained for the film.

The surface of the sample was observed through a scanning electron microscope to find surface irregularities at a magnification of about 8,000, but free of minute holes. The film was therefore evaluated as a favorable insulator coating.

In the step corresponding to FIG. 3(F), the interlayer insulator 41 was formed by depositing a silicon oxide film by sputtering mentioned hereinbefore. Alternatively, the silicon oxide film may be deposited using an LPCVD or a photochemical vapor deposition method. The silicon oxide film thus obtained was 0.2 to 1.0 μm thick. Then, as is also shown in FIG. 3(F), a contact hole 42 was perforated in the film using a photomask ⑤. This fabrication process according to the present invention is

characterized by that a reactive ion etching (RIE) process was employed to perforate the contact hole 42 at a position as near as possible to the channel, using gate electrodes 25 and 26 and the aluminum oxide film around them in a self-aligned manner, and thus minimizing the distance L between the channel and the feeding points for the source and the drain.

Then, aluminum was deposited over the whole structure by sputtering at a thickness of 0.5 to 1.0 μm, and leads 52 and 53 were formed using a photomask ⑥. These leads were used as contacts for the source regions 28 and 35 of the P-TFT and the N-TFT as shown in FIG. 3(G).

The surface of the resulting structure was coated with an organic resin 44, e.g., a transparent polyimide resin for smoothening, and subjected again to perforation of contact holes using a photomask ⑦.

As is shown in FIG. 3(G), two TFTs were brought into a complementary arrangement, and an output terminal thereof was connected to a transparent electrode 43 provided to one side of a pixel of a liquid crystal device. The transparent electrode 43 was fabricated by etching an indium tin oxide (ITO) film having established by sputtering, using a photomask ⑧ at the etching. The ITO film was such having deposited in a temperature range of from room temperature to 150°C, followed by annealing at 200 to 400°C in oxygen or in the atmosphere. Thus was fabricated a structure comprising the P-TFT 21, the N-TFT 22, and the transparent electrode 43 made of a conductive film on a single glass substrate 1.

The TFT thus obtained comprises a P-TFT having a mobility of 20 $cm^2/Vsec$ with a V_{th} of -5.9 V, and an N-TFT having a mobility of 40 $cm^2/Vsec$ with a V_{th} of +5.0 V.

It can be seen from the foregoing description that a mobility far higher than a value generally believed for a TFT has

been achieved. This has enabled for the first time the production of an active matrix liquid crystal display device using a C/TFT pair for each of the pixels of the liquid crystal electro-optical device. Furthermore, the present invention has also enabled formation of the peripheral circuits on-glass, i.e., by fabricating the circuits on the same substrate employing a fabrication process similar to that applied to the fabrication of the TFTs.

In the EXAMPLE, the TFT according to the present invention was applied to a liquid crystal electro-optical device. Because of the excellent frequency characteristics of the TFTs, such liquid crystal electro-optical devices can easily display dynamic images, and are therefore suitable for applications such as projection TV sets, view finders of video movies, and hanging-type TV sets. Additional application field to be mentioned is the driving elements of one- and two-dimensional image sensors, in which the excellent frequency characteristic is taken full advantage of in the rapid reading that can fully respond to the G4 standard.

A cell for a liquid crystal electro-optical device can be fabricated by a process well known in the art, using a pair of glass substrates, one having fabricated in a manner described above and the other having established thereon counter electrodes composed of transparent electrodes provided in stripes. The glass cell is filled with a liquid crystal material. If a twisted nematic (TN) liquid crystal were to be used, the cell spacing should be controlled to be about 10 μm, and orientation control films formed by rubbing treatment should be provided on the both of the transparent conductive films.

If a ferroelectric liquid crystal (FLC) were to be used as the liquid crystal material instead, the operating voltage should be controlled to ± 20 V, the cell spacing should be controlled to

1.5 to 3.5 μm, e.g., 2.3 μm, and the orientation control film should be formed only on the counter electrode by subjecting the film to rubbing treatment.

In the case a dispersion type liquid crystal or a polymer liquid crystal is used, an orientation control film can be omitted and the operation voltage should be controlled to ±10 to ±15 V and the cell spacing to 1 to 10 μm to increase the switching rate.

Since the polarizer sheet can be excluded particularly in the case a dispersion type liquid crystal is used, the cell can be used either as a reflection type or as a transmission type and have an increased quantity of light. Moreover, because the liquid crystal has no threshold, the use of the C/TFT according to the present invention having a distinct threshold voltage enables a device having a higher contrast and free of cross-talk (undesired interference between the neighboring pixels).

EXAMPLE 2

Referring to FIG. 10, an example of an active matrix type liquid crystal electro-optical device to which a TFT according to the present invention is applied is described. FIG. 10 shows the circuit diagram of the liquid crystal electro-optical device, and it can be seen therefrom that the active elements of the present EXAMPLE are provided in a complementary arrangement having a P-TFT and an N-TFT per one pixel contact.

The actual arrangement of the contacts and the like corresponding to the circuit shown in FIG. 10 is given in FIG. 12. For brevity's sake, merely a part of the circuit corresponding to a 2 x 2 matrix is given in FIG. 12.

Referring first to FIG. 11, the process for fabricating the substrate for use in the liquid crystal electro-optical device according to the present invention is described. FIG. 11(A) shows

a step of depositing silicon oxide film as a blocking layer 151 at a thickness of from 1000 to 3000 Å, on a non-expensive glass substrate 150 using RF magnetron sputtering. In this case, the glass substrate is made of a non-expensive glass which resists to a heat treatment at 700°C or lower, e.g., at about 600°C. The conditions for the fabrication are the same as those used in EXAMPLE 1. An amorphous silicon film was formed on the blocking layer at a thickness of 500 to 3000 Å, e.g. 1500Å in the same way as in the EXAMPLE 1. Then, the amorphous silicon film was annealed in, for example, hydrogen atmosphere at 600°C for a duration of 12 to 70 hours.

The amorphous silicon film turned into a phase having a higher structural ordering upon annealing, comprising partly a crystalline portion. The resulting film had a hole mobility, μh, of from 10 to 200 $cm^2/V \cdot sec$, and an electron mobility, μe, of from 15 to 300 $cm^2/V \cdot sec$.

As is shown in FIG. 11(A), the silicon film was subjected to a photoetching treatment using a first photomask (11) to establish a P-TFT area 130 (having a channel length of 20 μm) and an N-TFT area 140, at the left and the right hand side, respectively, of FIG. 11(A).

On the resulting structure was deposited a silicon oxide film as a gate insulating film 153 to a thickness of from 500 to 2,000 Å, e.g., to a thickness of 700 Å. The conditions for the film deposition were the same as those employed in depositing the silicon oxide film 151 which gave a blocking layer. Further, a small amount of fluorine may be added during the film deposition to fix sodium ions. In this EXAMPLE, a silicon nitride film 154 was deposited on the gate insulating film as a blocking layer to avoid reaction of the gate insulating film and the gate electrode to be formed thereon. This silicon nitride film had a thickness of from 50 to 200 Å, more specifically, 100 Å.

Further on the structure thus obtained above was deposited an aluminum film as a gate electrode material at a thickness of from 3,000 Å to 1.5 μm, 1 μm for example, by a known sputtering process.

Other useful materials for the gate electrode include molybdenum (Mo), tungsten (W), titanium (Ti), tantalum (Ta), and alloys thereof with silicon, as well as laminate wires of silicon with other metal films.

The use of a metal as the gate electrode, particularly, aluminum or a like material having a low resistance as in the present EXAMPLE, avoids gate delay (delay in the pulsed voltage which is transferred through the gate wire and distortion of the waveform) which becomes more pronounced with increasing area and finer patterning of the substrate, and hence facilitates fabrication of devices with a large-area substrate.

The aluminum film thus deposited was patterned through a second photomask (12) to obtain a structure as shown in FIG. 11(B), having a gate electrode 155 for the P-TFT and a gate electrode 156 for the N-TFT. Both of the gate electrodes were connected to a common gate wire 157.

The substrate was immersed into an AGW electrolyte having prepared by adding 9 parts of propylene glycol to 1 part of an aqueous 3% tartaric acid solution. A direct current (D.C.) was applied to the substrate by connecting the aluminum gate to the anode of a power source and using a platinum cathode as the counter electrode. The gate electrodes were each connected to the respective gate wires, and a connection terminal was provided at the vicinity of the substrate end to clamp all the gate wires therewith for the connection. The anodic oxidation was conducted in this manner to form anodically oxidized films 158 and 159 around the gate electrodes as is shown in FIG. 11 (C).

In the anodic oxidation process, the electric current was

applied first at a constant current density of 4 mA/cm^2 for 20 minutes, and then at a constant voltage for 15 minutes, to thereby obtain a 2,500 Å thick aluminum oxide film around the gate electrode. It is preferred to form the anodic oxide film as thick as possible, and this approach was taken in the present EXAMPLE as far as the process conditions permit.

As is shown in FIG. 11(D), the nitride film 154 and the silicon oxide film 153 on the semiconductor was removed by etching. Then, boron was doped over the whole substrate as an impurity for P-TFT, at a dose of from 1×10^{15} to $5 \times 10^{15} cm^{-2}$ by ion implantation. The concentration of the doping was controlled to about 10^{19} atoms·cm^{-3} to establish a source 160 and a drain 161 for the P-TFT. In the present EXAMPLE, the ion doping was conducted after removing the insulator films on the surface. However, it is also possible to conduct the doping through the insulator films 153 and 154, by changing the conditions of ion implantation.

Similarly, as shown in FIG. 11(E), a photoresist 464 was formed using a third photomask (13) to cover the P-TFT area, and phosphorus was doped by ion implantation to establish a source 162 and a drain 163 for the N-TFT. The phosphorus was added at a dose of from 1×10^{15} to $5 \times 10^{15} cm^{-2}$, so that the doping concentration became about 10^{20} atoms·cm^{-3}. In this case, an oblique doping was used, in which the ion was bombarded obliquely to the substrate in such a manner that the direction of the ion beam may make an acute angle with respect to the surface of the substrate. This process allows the impurity ions to intrude into a lower portion under the anodic oxide film around the gate. In this manner, the ends of the source and the drain areas were roughly adjusted to match the end of the gate electrode. Thus, the anodically oxidized film can function sufficiently as an insulator to the contact wiring to be formed in the later steps.

and hence excludes a step of forming an insulator film.

The structure was then re-heated at 600°C for a duration of 10 to 50 hours for annealing. Thus, the doped impurities in the source 160 and the drain 161 of the P-TFT, as well as those in the source 162 and the drain 163 of the N-TFT were activated to give P^+ and N^+. Under the gate electrodes 155 and 156 were formed channel forming regions 164 and 165. Instead of employing thermal annealing for the activation as in the present EXAMPLE, a laser beam may be irradiated to the source and the drain regions for the activation. In such a case, the activation can be performed in an instant and therefore the problem of thermal diffusion of the gate metal need not be considered. Accordingly, it is possible to omit the formation of silicon nitride film 154 which functions as a blocking layer on the gate insulating film.

A silicon oxide film as an insulator film was then deposited on the surface of the resulting structure by sputtering as mentioned above. The film is preferably as thick as possible, e. g., in a range of from 0.5 to 2.0 μm, 1.2 μm in this EXAMPLE. The film is then subjected to anisotropic etching from the upper side thereof to form a remainder area 166 at the vicinity of the side walls of a protrusion composed of the gate accompanied by the anodically oxidized film. The resulting structure is given in FIG. 11(F).

Then, the unnecessary portions were removed from the semiconductor film 152 by etching, using the protrusion above and the remainder area 166 as the mask. Then, the remainder area 166 around the protrusion was removed. Thus were obtained exposed semiconductor portions 152 at the outer side of the protrusion so that they may become a source and a drain region for each of the TFTs. The resulting structure is given in FIG. 11(G).

The whole structure was then covered with aluminum by sputtering, and after patterning the aluminum film through a

fourth mask (14) to obtain leads 167 and 168 and contact portions 169 and 170, the unnecessary semiconductor film sticking out was removed by etching from the contacts 167, 168, 169, and 170; the gate electrodes 155 and 156; and the anodic oxide films 158 and 159 which accompany the gate electrodes. Thus were the elements separated from each other to complete a TFT. It can be seen from the foregoing description that a C/TFT pair was fabricated using merely four masks. The C/TFT pair thus obtained is shown in FIG. 11(H).

The TFT thus obtained comprises a gate electrode completely covered with an anodically oxidized film, and all the parts, exclusive of the source and the drain regions having contact connections sticking out from the gate portion, are established under the gate. The source and the drain electrodes are in contact with the source and the drain regions at two points, i.e., at the upper surface and the side face, to assure a sufficient ohmic contact.

Thus, as described in the foregoing, a C/TFT can be fabricated without heating the structure to a temperature 700°C or higher through the whole process. Thus, an economically advantageous substrate can be used instead of an expensive one such as of quartz, and hence the process is best suited for producing liquid crystal electro-optical devices of many pixels.

The thermal annealing was conducted twice in the present EXAMPLE, as shown in FIGS. 11(A) and 11(E). However, the annealing corresponding to that of FIG. 11(A) may be omitted depending on the required device characteristics, and the thermal annealing may be integrated into one corresponding to that of FIG. 11(E) to speed up the process. Furthermore, the silicon nitride film 154 provided under the aluminum gate efficiently avoided reaction of the aluminum gate with the gate insulating film under the gate, and a favorable interfacial characteristic

was realized.

Then, an ITO film was deposited by sputtering between two TFTs, so that the output contact thereof may be connected to a liquid crystal device, through one of the pixel electrodes provided as a transparent electrode in a complementary structure. The ITO film was deposited in the temperature range of from room temperature to 150°C, which was annealed at 200 to 400°C in oxygen or in the atmosphere. The ITO film thus obtained was etched through a fifth photomask (15) to provide a pixel electrode 171. The resulting structure comprised a glass substrate having provided thereon a P-TFT 130, an N-TFT 140, and a transparent electrode 171 made from a transparent conductive film. The TFT thus obtained comprises a P-TFT having a mobility of 20 $cm^2/Vsec$ with a V_{th} of -5.9 V, and an N-TFT having a mobility of 40 $cm^2/Vsec$ with a V_{th} of +5.0 V.

In FIG. 12 is given the arrangement of the electrodes and the like of this liquid crystal electro-optical device. The cross sectional view along the line C-C' in FIG. 12 corresponds to those given in FIG. 11. The P-TFT 130 is provided to the crossing point of a first signal wire 172 and a third signal wire 157. Similarly, a P-TFT for another pixel is provided to the crossing point of the first signal wire 172 and another third signal wire 176 established as a right side neighbor of the wire 157. The N-TFT, on the other hand, is provided to the crossing point of a second signal wire 173 and the third signal wire 157. Furthermore, a P-TFT for another pixel is provided to the crossing point of another first signal wire 174 neighboring on the wire 172 and a third signal wire 157. Thus was obtained a matrix structure constructed from C/TFTs. The P-TFT 130 is connected to the first signal wire 172 through the contact of the drain 161, and the gate 155 is connected to the signal wire 157. The output terminal of the source 160 is connected to the pixel

electrode 171 through a contact.

Similarly, the N-TFT 140 is connected to the second signal wire 173 through the contact of the source 162, to the signal wire 157 through the gate 156, and to the same pixel electrode 171 as in the case of P-TFT, by the output terminal of the drain 163 through a contact. Another C/TFT, which is provided next to the one described above and connected to the same third signal wire above, comprises a P-TFT 131 connected to the first signal wire 174 and an N-TFT 141 connected to a second signal wire 175. In this manner a pixel 180 is constructed inside a pair of signal wires 172 and 173, comprising a pixel electrode 171 composed of a transparent conductive film and a C/TFT pair. By repeating this structure along the vertical and horizontal directions, a 2 x 2 matrix can be extended into liquid crystal electro-optical devices having many pixels, such as those composed of 640 x 480 pixels and 1280 x 960 pixels. In the foregoing description, the impurity doped regions of the TFTs are referred to as source and drain for making the explanation simple. In the actual drive of the TFTs, the functions of those regions may differ in some cases.

In the TFT of the present EXAMPLE, the elements in each of the TFTs are separated into islands by removing the semiconductor film 152 through an etching process using a first photomask. Accordingly, the gate wiring outside the TFT areas is free of the underlying semiconductor film, and is established on the substrate or an insulator film having formed on the substrate. This structure avoids formation of a capacitance at the gate input side, and allows a high speed response.

A liquid crystal electro-optical device was then fabricated using the thus obtained substrate having established thereon the active elements. The substrate was first screen-coated with a UV-curable epoxy-modified acrylic resin having dispersed therein

50 % by weight of a nematic liquid crystal. In the process, a 125 mesh/inch screen was used for the coating, and a squeegee pressure of 1.5 kg/cm^2 was applied. The resulting emulsion thickness was 15 μm. After leveling for 10 minutes, the resin emulsion layer was cured with a high pressure mercury vapor lamp emitting a light having the main peak at a wavelength of 236 nm at an energy of 1,000 mJ. Thus was obtained a 12 μm thick light influencing layer.

A second electrode was then established on the cured resin layer by depositing thereon a 2,500 Å thick molybdenum (Mo) film by D.C. sputtering.

A black-colored epoxy resin was then applied to the surface by screen-printing, which was pre-baked at 50°C for 30 minutes and then baked at 180°C for 30 minutes to establish a 50 μm thick protective film.

A reflection-type liquid crystal display device was completed by connecting a TAB-shaped driver IC to the lead on the substrate. This device was comprises only one substrate.

In the EXAMPLE described above, a pair of TFTs in a complementary arrangement was provided as an active element to each of the pixels. However, the liquid crystal electro-optical devices are not limited to this structure, and plural pairs of TFTs in a complementary arrangement may be provided to each of the pixels. Otherwise, plural pairs of TFTs in a complementary arrangement may be provided to pixel contacts divided into plural contacts.

A liquid crystal electro-optical device comprising a dispersion type liquid crystal equipped with active elements was completed in this manner. Since the dispersion-type liquid crystal of the present EXAMPLE can be constructed on only one substrate, a light-weight and thin liquid crystal electro-optical device can be realized economically. More advantageously, a

liquid crystal electro-optical device of high illuminance was obtained, because the device is constructed from a single substrate free of polarizer sheets and orientation control films.

EXAMPLE 3

Referring to FIG. 13, an example of a liquid crystal electro-optical device comprising pixels having provided to each thereof modified transfer-gate TFTs in a complementary arrangement is described. The TFTs in this EXAMPLE are fabricated basically in the same process as those in EXAMPLE 2, and the process steps proceed in a similar manner as shown in FIG. 11. The only difference is the arrangement of the C/TFT shown in FIG. 11, because the one used in the present EXAMPLE is a modified transfer-gate C/TFT. The actual arrangement and connection of the C/TFT of the present EXAMPLE is given in FIG. 14.

As shown in FIG. 13, a common gate wire 191 is connected with gates of a P-TFT 195 and a N-TFT 196. These TFTs are connected to another signal wire 193 through source and drain areas, and the other source and drain areas are connected to a common pixel electrode.

The fabrication process proceeds the same to FIG. 11(G). The structure obtained to the step shown in FIG. 11(G) is coated with a silicon nitride film 200 at a thickness of from 500 to 2,000 Å. The resulting silicon nitride film 200 is anisotropically etched along the direction vertical to the substrate to remain the silicon nitride film on the side wall of the anodically oxidized film 201 provided on the gate electrode. The silicon nitride film need not be left out uniformly, provided that the film remains at least on the gate 207 and on the gate insulating film at the proximity of the semiconductor. This silicon nitride film 200 functions as a protective layer to avoid short circuit at the vicinity of the end portion of a gate insulating film 203, caused

by a metallic wiring 202, a source area 204, and a drain area 205, upon formation of source and drain 202 at the later steps.

On the surface of the resulting structure is then deposited an interlayer insulator film and a silicon oxide film 206 at a thickness of from 1,000 Å to 2 μm, e.g., 6,000 Å in this case. After forming a photoresist thereon, a mask is formed on the gate 207 using the gate as the mask by exposure to light from the substrate side. Then an interlayer insulator film 206 can be obtained on the gate by etching.

The process is then forwarded in the same manner as in FIGS. 11(H) and 11(I), to thereby complete the structure into a modified transfer-gate TFT having an arrangement and structure as shown in FIGS. 14(A), 14(B), and 14(C). In FIGS. 14(B) and 14(C) are shown clearly that the gate 207 always comprises thereon an interlayer insulator film 206, by which an effective interlayer insulating function is provided to the crossings of the lead portion of the gate wiring 207 with the lead portion of the source and drain wiring 202. Thus, as is shown in FIG. 14(A), the formation of unfavorable wiring capacitance could be avoided.

As was described above, an active element substrate was obtained with the same number of masks as that in EXAMPLE 2, yet having reduced in capacitance around the wiring and composed of TFTs having such a structure less apt to cause short circuit at the vicinity of the gate insulating film.

An active matrix super-twisted nematic (STN) liquid crystal electro-optical device was then produced, by combining and adhering the substrate obtained above as a first substrate with a second substrate having subjected to orientation treatment and having provided thereon a counter electrode, and injecting an STN liquid crystal therebetween according to a known technology.

In the foregoing EXAMPLES, the TFTs according to the present invention were applied to liquid crystal electro-optical devices.

However, the EXAMPLES above are not limiting, and the TFTs can be readily applied to other devices and three-dimensional IC elements and the like.

The present invention enables fabrication of TFT elements using considerably reduced number of masks. Accordingly, semiconductor devices can be produced through a far simpler fabrication process and with increased production yield by applying the TFTs of this structure to the fabrication of the devices. Thus, the present invention provides semiconductor devices at a reduced production cost.

The TFT according to the present invention comprises a metallic gate electrode having subjected to anodic oxidation to form an oxide film on the surface thereof, so that a wiring comprising a three-dimensional crossing can be established thereon. Furthermore, the feeding points of the source and the drain are provided very near to the channel by the use of said gate with an oxide film around it, and by exposing only the contact portions of the source and the drain out of the gate. Thus were avoided the drop of frequency characteristics of the device and the increase of ON resistivity.

Furthermore, in an embodiment according to the present invention in which an aluminum gate is used, hydrogen having incorporated into the gate oxide film could be reduced during the annealing step by dissociating H_2 into H taking advantage of the catalytic effect of aluminum. Thus, the interfacial density of states (Q_{SS}) could be lowered as compared to the case in which a silicon gate is used, and, by this effect, an element having improved characteristics was realized.

The source and the drain of the TFTs according to the present invention were established in a self-aligned manner. The same was done in the positioning of contact portions of the source and the drain. Thus, the area necessary to accommodate the

elements to construct a TFT was reduced, and hence was effective for achieving a higher degree of integration. In the case the TFTs were used as active elements for a liquid crystal electro-optical device, the aperture ratio of the liquid crystal panel was increased.

The anodically oxidized film around the gate was taken full advantage of, and a TFT having a distinguished structure was proposed. This TFT, moreover, can be fabricated with minimized number of masks, the minimum being 2 masks.

In a C/TFT according to the present invention, a semi-amorphous or semi-crystalline semiconductor was used. However, the semiconductor may be replaced by semiconductors differing in crystal structure if possible, provided that they are used for the same purpose. By the use of a self-aligned C/TFT, a rapid processing was possible. However, this is not limiting, and TFTs may be fabricated by a non-self-aligned manner without using ion implantation. Furthermore, it should be noted that the present invention is not limited only to stagger-type TFTs, but also encompasses inverted-type stagger TFTs and other types of TFTs.

While the invention has been described in detail and with reference to specific embodiments thereof, it will be apparent to one skilled in the art that various changes and modifications can be made therein without departing from the spirit and scope thereof.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

source and drain semiconductor regions;

a gate electrode comprising a metal;

a channel located adjacent to said gate electrode between said source and drain semiconductor regions;

a gate insulating layer provided between said gate electrode and said channel;

source and drain electrodes connected to the source and drain semiconductor regions, respectively; and

an oxide layer comprising said metal and provided on a side of said gate electrode,

wherein a side of at least one of said source and drain electrodes is substantially aligned with a side of said oxide layer.

2. The semiconductor device of claim 1 wherein sides of both of said source and drain electrodes are substantially aligned with sides of said oxide layer.

3. The semiconductor device of claim 1 wherein said oxide layer extends on an upper surface of said gate electrode.

4. The semiconductor device of claim 1 wherein said oxide layer is in contact with said gate electrode and said at least one of said source and drain electrodes.

5. The semiconductor device of claim 1 wherein a side of corresponding one of said source and drain semiconductor regions is aligned with said side of said oxide layer.

6. The semiconductor device of claim 1 wherein said gate

electrode is distant from corresponding one of said source and drain semiconductor regions substantially by a thickness of said oxide layer in a direction from said source semiconductor region to said drain semiconductor region.

7. The semiconductor device of claim 1 wherein said oxide layer is formed by oxidizing the metal of a peripheral portion of said gate electrode.

8. A semiconductor device comprising:

source and drain semiconductor regions;

a gate electrode comprising a metal;

a channel located adjacent to said gate electrode between said source and drain semiconductor regions;

a gate insulating layer provided between said gate electrode and said channel;

source and drain electrodes connected to the source and drain semiconductor regions at side and upper surfaces of said source and drain semiconductor regions, respectively; and

an oxide layer comprising said metal and provided between said gate electrode and said source and drain electrodes.

9. The semiconductor device of claim 8 wherein said oxide layer extends on an upper surface of said gate electrode and said source and drain electrodes extend on an upper surface of said oxide layer.

10. The semiconductor device of claim 8 wherein said source and drain semiconductor regions and said channel are located in a semiconductor layer provided on a substrate and said source and drain electrodes are provided on said substrate and said side surfaces of said source and drain semiconductor regions are side

surfaces of said semiconductor layer.

11. The semiconductor device of claim 8 wherein said gate electrode is distant from said source and drain semiconductor regions substantially by a thickness of said oxide layer in a direction from said source semiconductor region to said drain semiconductor region.

12. The semiconductor device of claim 8 wherein said oxide layer is formed by oxidizing the metal of a peripheral portion of said gate electrode.

13. A method for forming a semiconductor device comprising the steps of:

forming a semiconductor film on a substrate;

forming a gate electrode comprising a metal on said semiconductor film with a gate insulating layer therebetween; and

oxidizing said metal of a peripheral portion of said gate electrode to form an oxide of said metal at least on a side surface of said gate electrode.

14. The method of claim 13 further comprising the steps of:

forming an insulating film on said substrate over said gate electrode; and

forming at least one contact hole on corresponding one of said source and drain semiconductor regions in said insulating film with a side surface of said contact hole located substantially on a side surface of said oxide.

15. The method of claim 14 wherein said contact hole forming step is carried out with said gate electrode and said oxide as a mask.

16. The method of claim 14 wherein said contact hole forming step is carried out to leave the insulating film on an upper surface of said gate electrode by the use of a photomask.

17. The method of claim 16 wherein the insulating film is left on said upper surface of said gate electrode with said oxide extending therebetween by said contact hole forming step.

18. The method of claim 13 wherein said semiconductor film forming step is carried out by forming a silicon semiconductor film containing hydrogen therein on said substrate and subsequently crystallizing said silicon semiconductor film by thermal treatment.

19. A method for forming a semiconductor device comprising the steps of:

forming a semiconductor film on a substrate;

forming a gate insulating layer on said semiconductor film;

forming a gate electrode comprising a metal on said gate insulating layer;

oxidizing said metal of a peripheral portion of said gate electrode by anodic oxidation to form an oxide of said metal at least in the vicinity of said semiconductor film;

forming an insulating film on said gate insulating layer over said gate electrode;

selectively removing the insulating film and the gate insulating layer by anisotropic etching to leave a portion of the insulating film and the gate insulating layer around a side of said gate electrode;

selectively removing the semiconductor film by etching

with said gate electrode and said oxide and the left portion of the insulating film as a mask;

exposing a portion of the semiconductor film provided under the left portion of the insulating film by removing the left portion of the insulating film and a portion of the gate insulating layer provided under the left portion of the insulating film by etching;

forming a conductive film on said substrate over said oxide and the exposed portion of the semiconductor film; and

patterning said conductive film with a mask to form source and drain electrodes which extend on said oxide and are in contact with upper and side surfaces of the exposed portion of the semiconductor film.

20. The method of claim 19 further comprising the step of implanting impurities into the exposed portion of the semiconductor film to form source and drain regions therein.

21. The method of claim 19 further comprising the step of implanting impurities into the semiconductor film with said oxide as a mask before said insulating film forming step.

22. A method for forming a semiconductor device comprising the steps of:

forming a semiconductor island on a substrate;

forming a gate insulating layer on said semiconductor island;

forming a gate electrode comprising a metal on said gate insulating layer;

oxidizing said metal of a peripheral portion of said gate electrode by anodic oxidation to form an oxide of said metal at least in the vicinity of said semiconductor island;

selectively removing the gate insulating layer with said gate electrode and said oxide as a mask;

forming an insulating film on said substrate over said oxide;

selectively removing the insulating film by anisotropic etching to leave a portion of the insulating film around a side of said gate electrode;

selectively removing the semiconductor island by etching with said gate electrode and said oxide and the left portion of the insulating film as a mask;

removing the left portion of the insulating film by etching to expose a portion of the semiconductor island provided under the left portion of the insulating film;

forming a conductive film on said substrate over the exposed portion of the semiconductor island; and

patterning said conductive film with a mask to form source and drain electrodes which extend on said oxide and are in contact with the exposed portion of the semiconductor island.

ABSTRACT

An insulated gate field effect semiconductor device comprising a substrate having provided thereon a thin-film structured insulated gate field effect semiconductor device, said device being characterized by that it comprises a metal gate electrode and at least the side thereof is coated with an oxide of the metal. The insulated gate field effect semiconductor device according to the present invention is also characterized by that the contact holes for the extracting contacts of the source and drain regions are provided at about the same position of the end face of the anodically oxidized film established at the side of the gate. Furthermore, the present invention provides a method for forming insulated gate field effect semiconductor devices using less masks.

Fig. 1

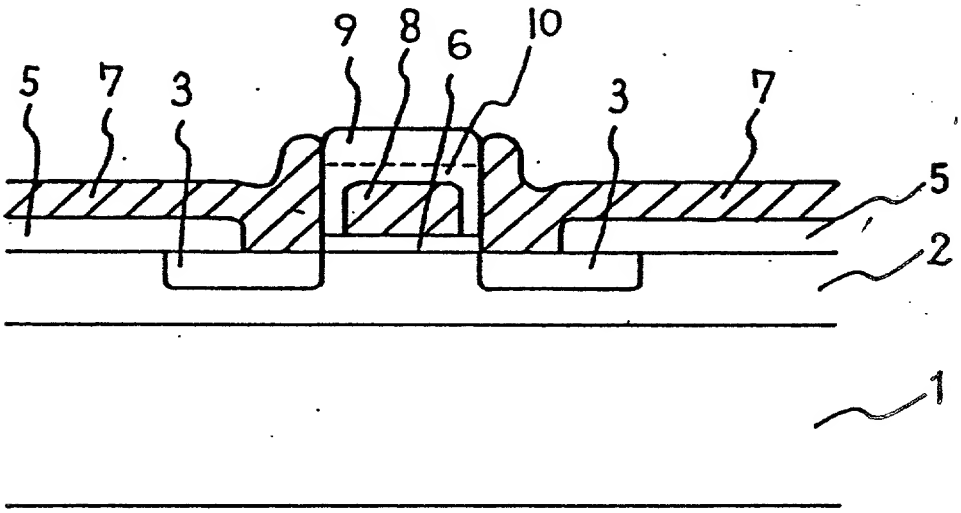


Fig. 2

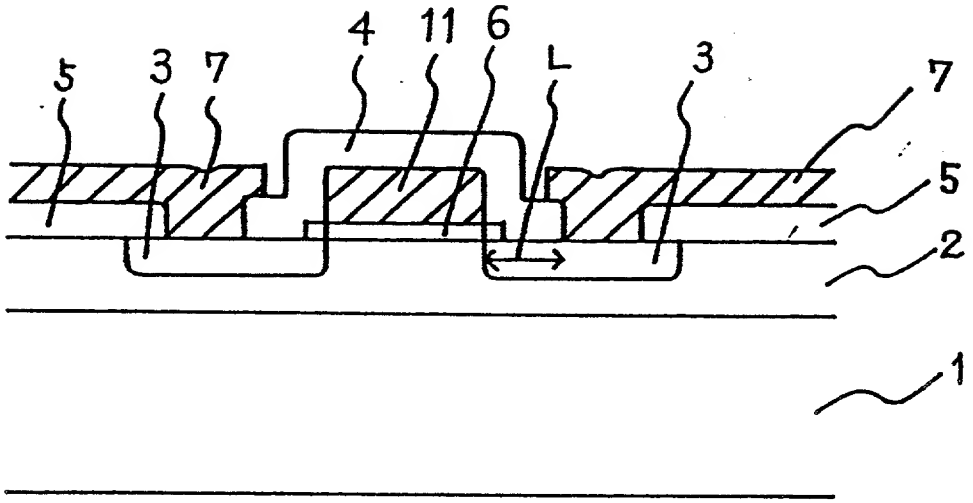
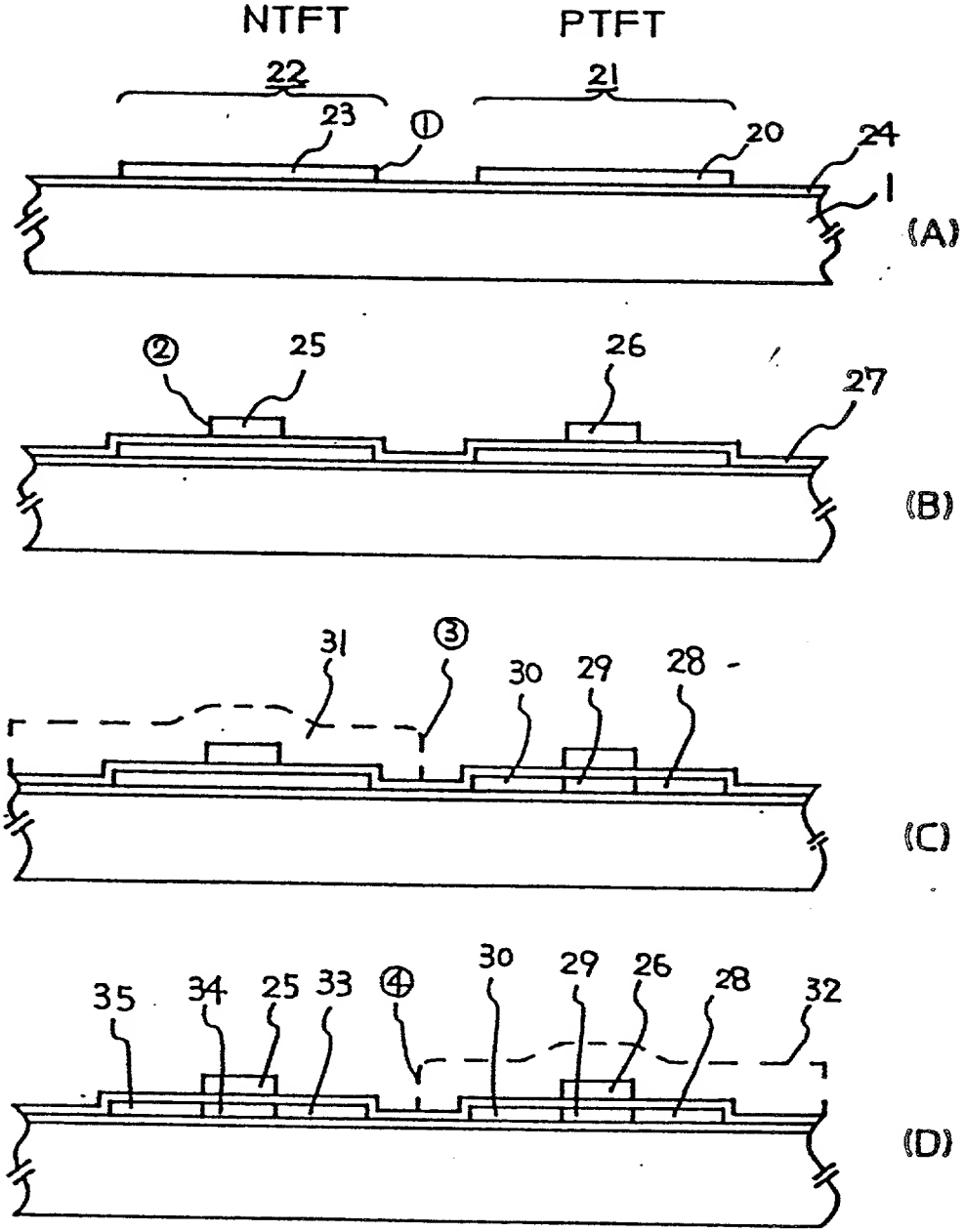


Fig. 3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PTFT
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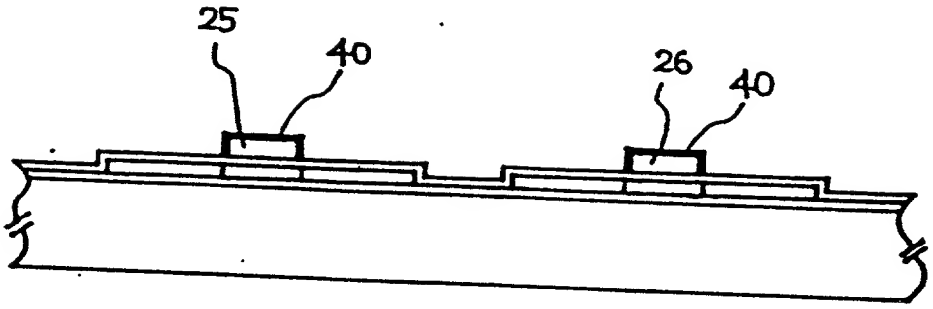
21
23
①
20
24
1
(A)
②
25
26
27
(B)
31
③
30
29
28
(C)
35
34
25
33
④
30
29
26
28
32
(D)

Fig. 3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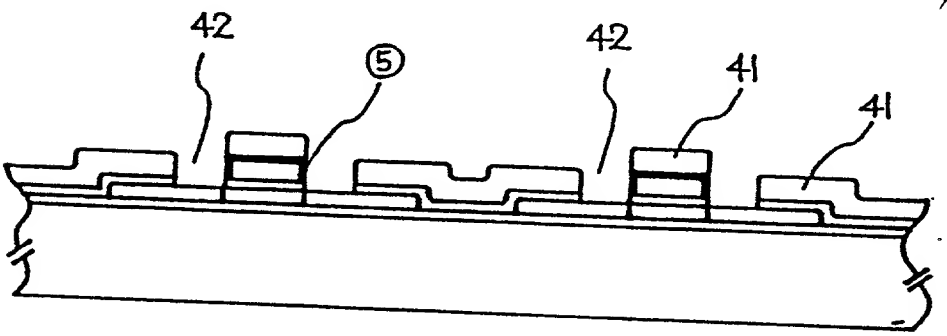
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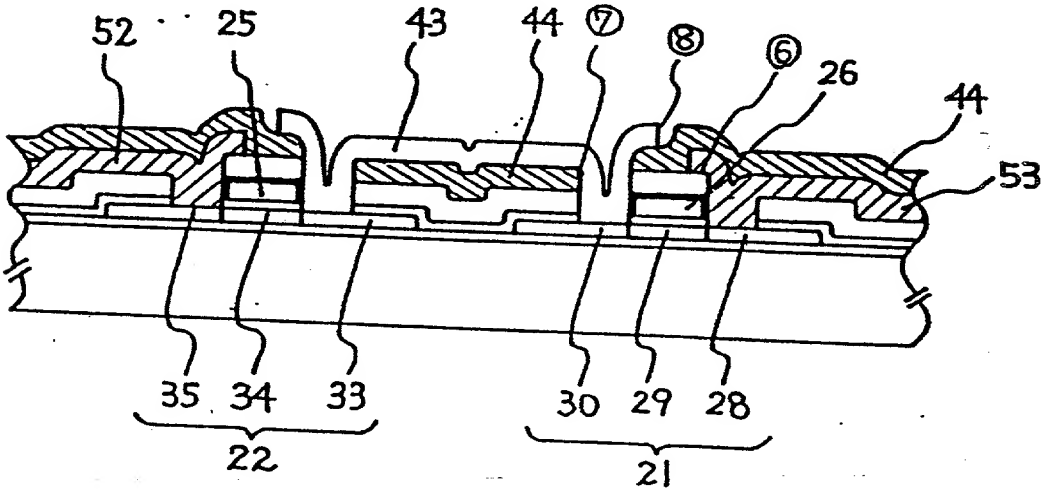
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25
43
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44
53
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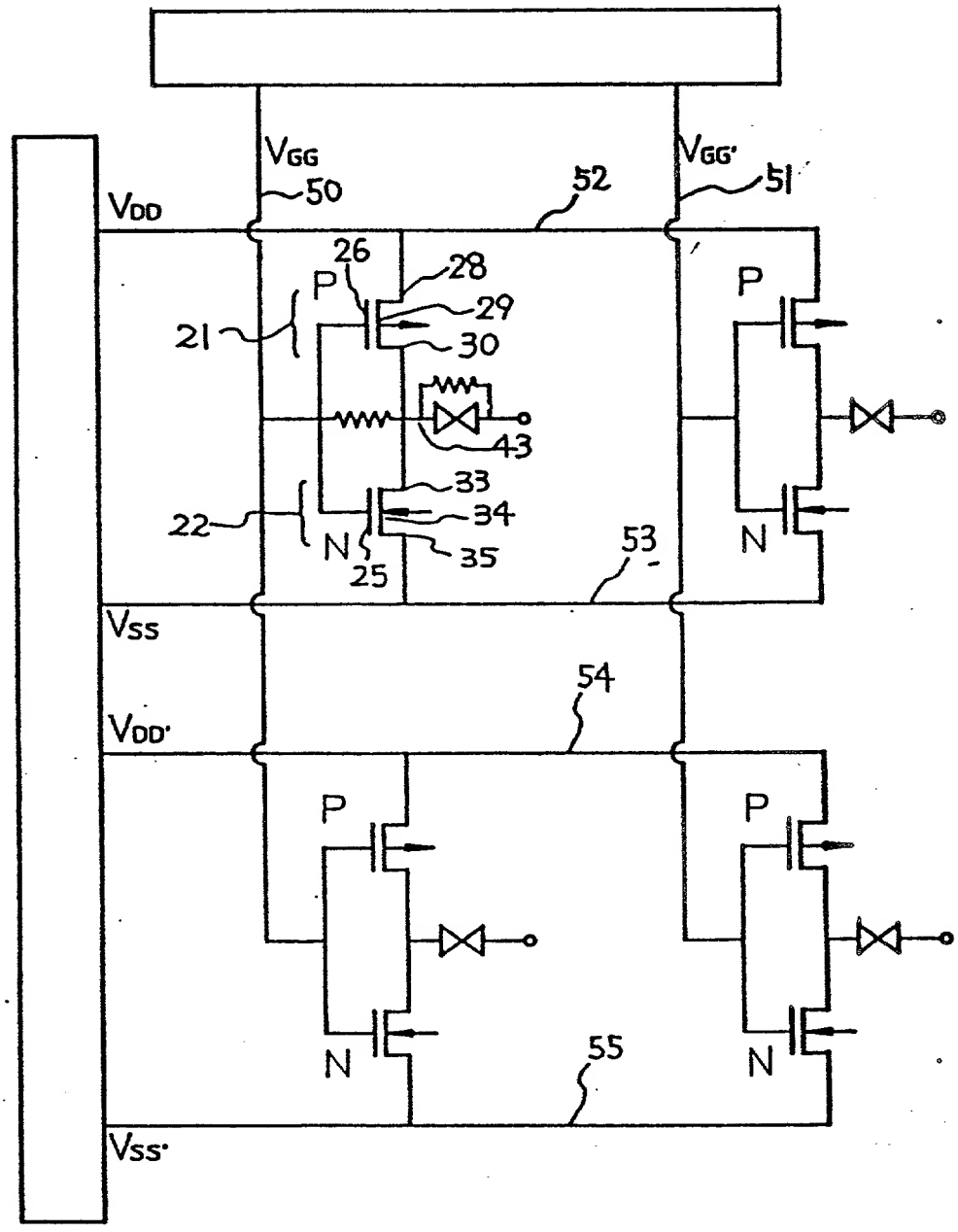
34
33
30
29
28
22
21

(G)

Fig. 4


VGG
50
52
VGG'
51
VDD
26
28
P
29
21
30
43
33
22
34
N
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35
53
P
N
Vss
54
VDD'
P
P
N
N
55
Vss'

Fig. 5

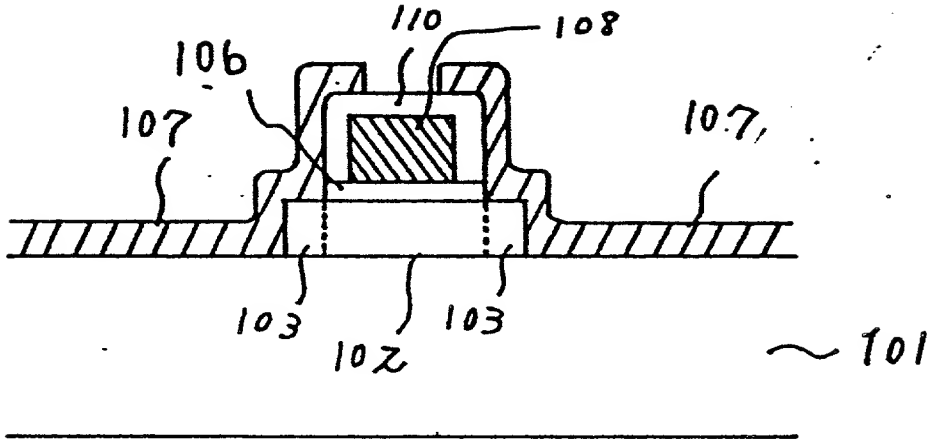


Fig. 6

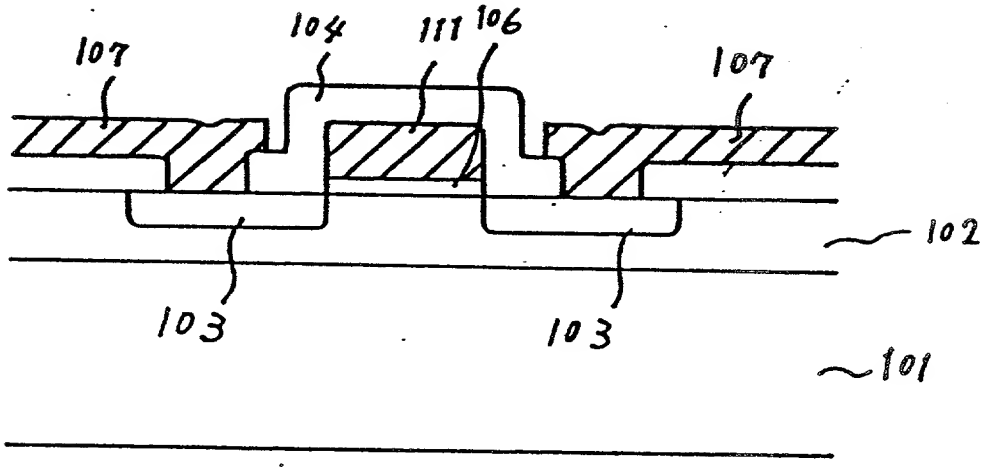
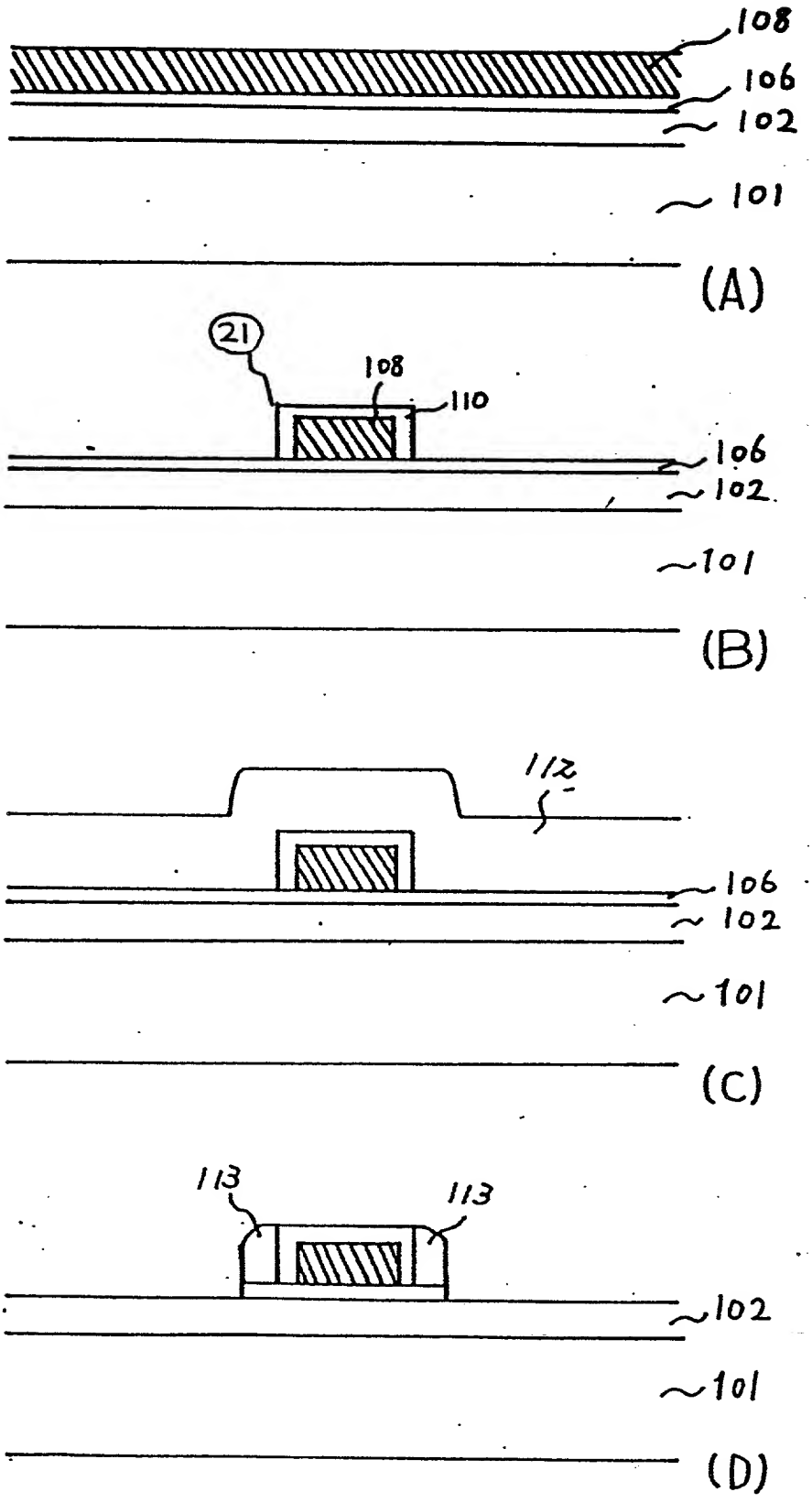


Fig. 7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(B)
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(C)
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113
102
101
(D)

Fig. 7

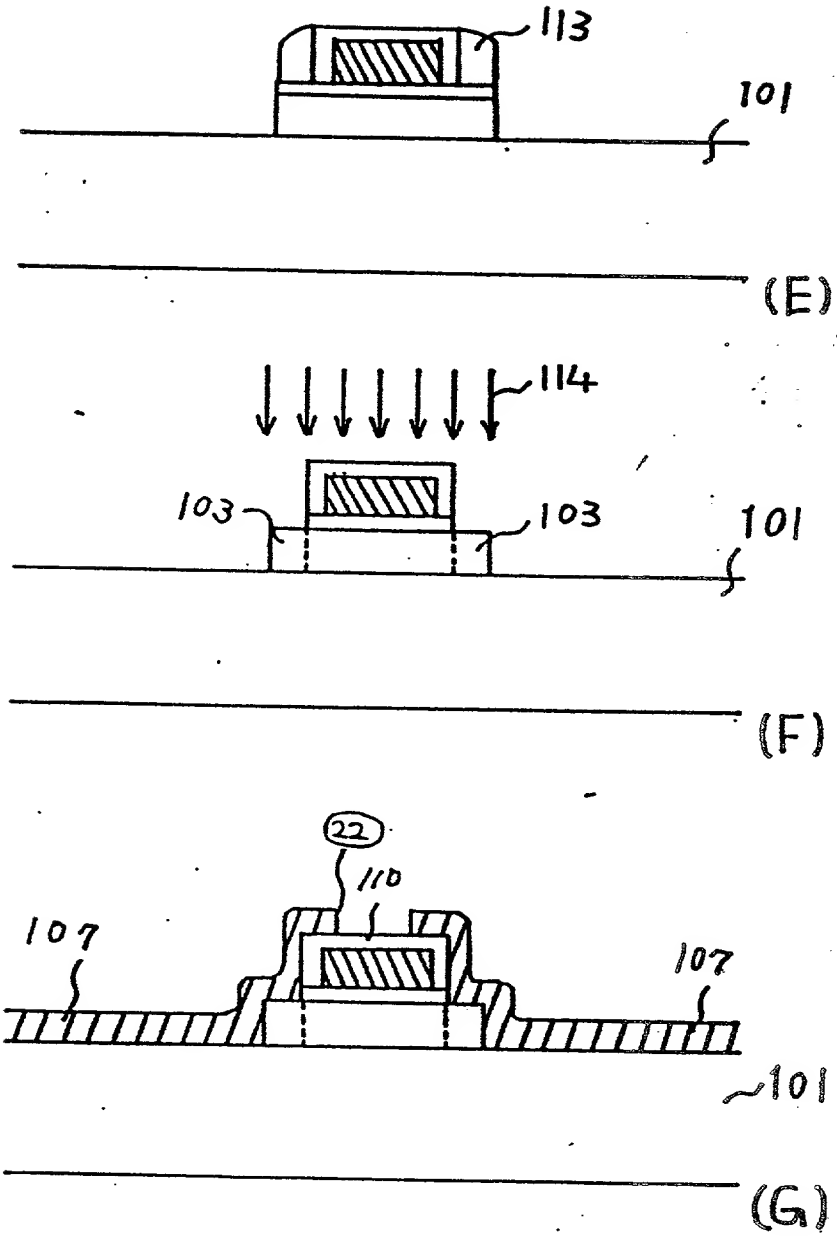
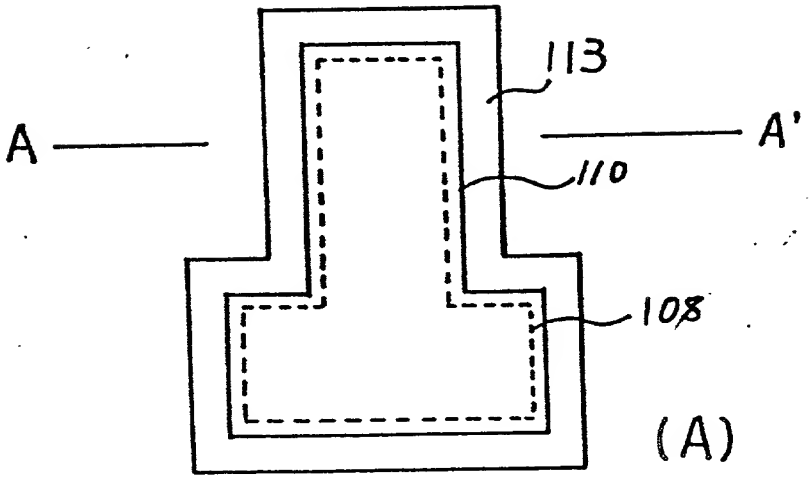


Fig. 8



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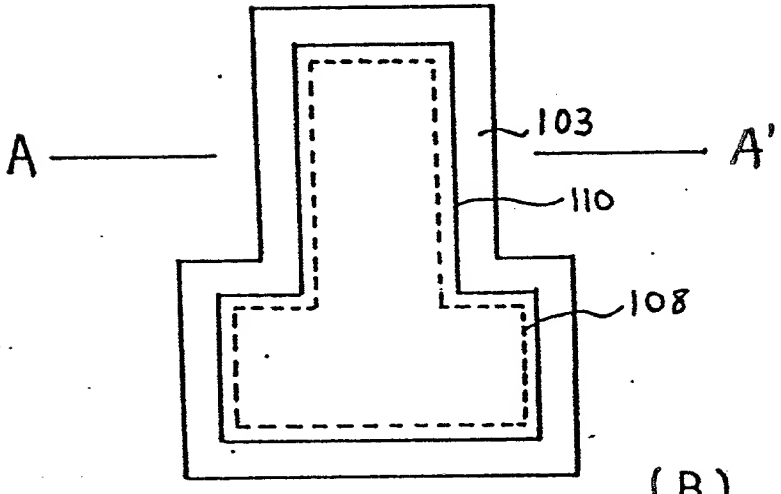
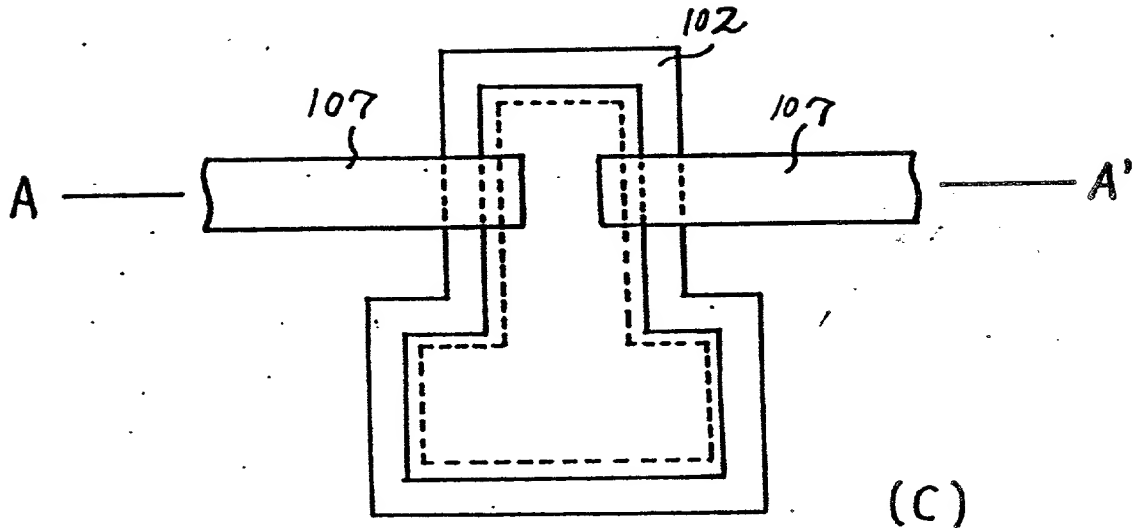


(B)

Fig. 8



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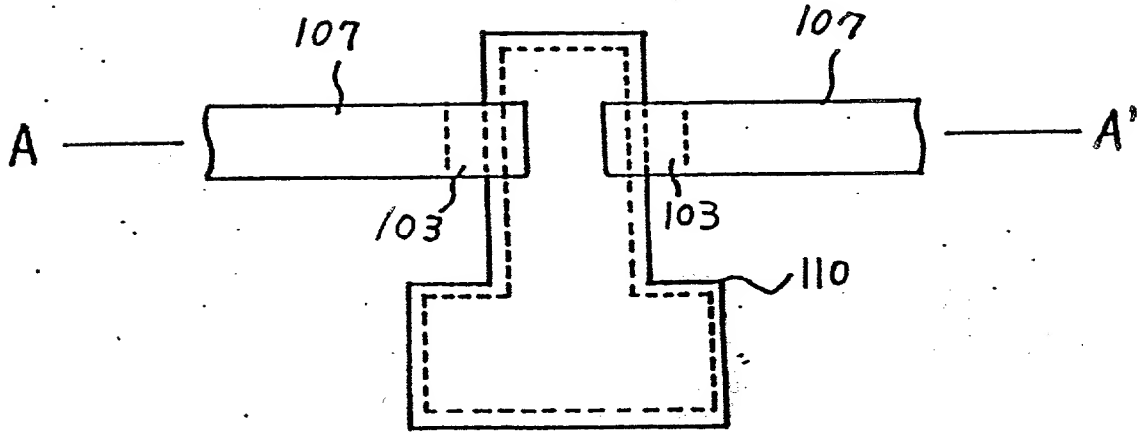
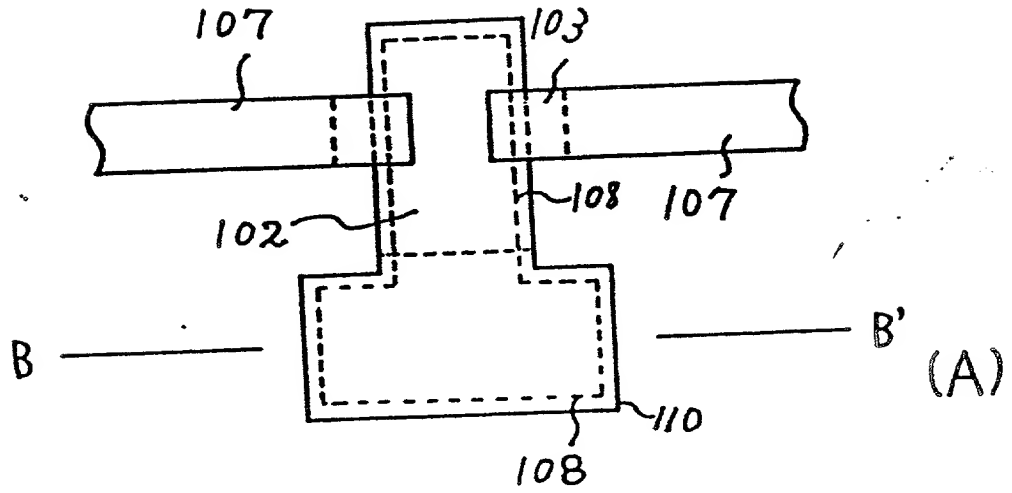


(D)

Fig. 9



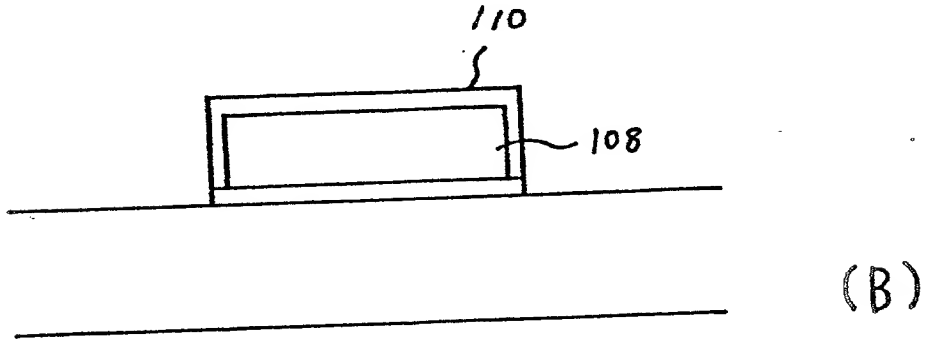
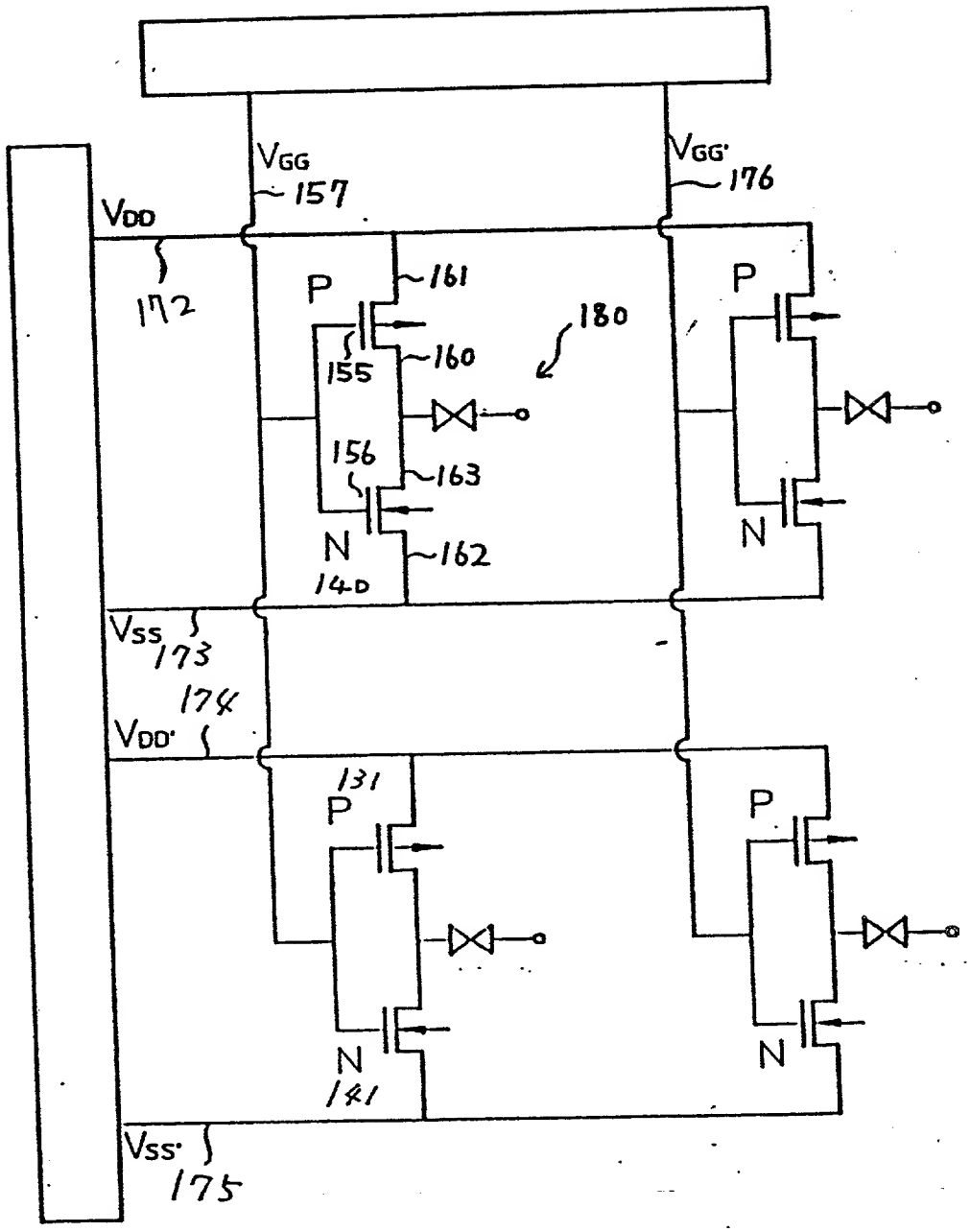


Fig. 10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141
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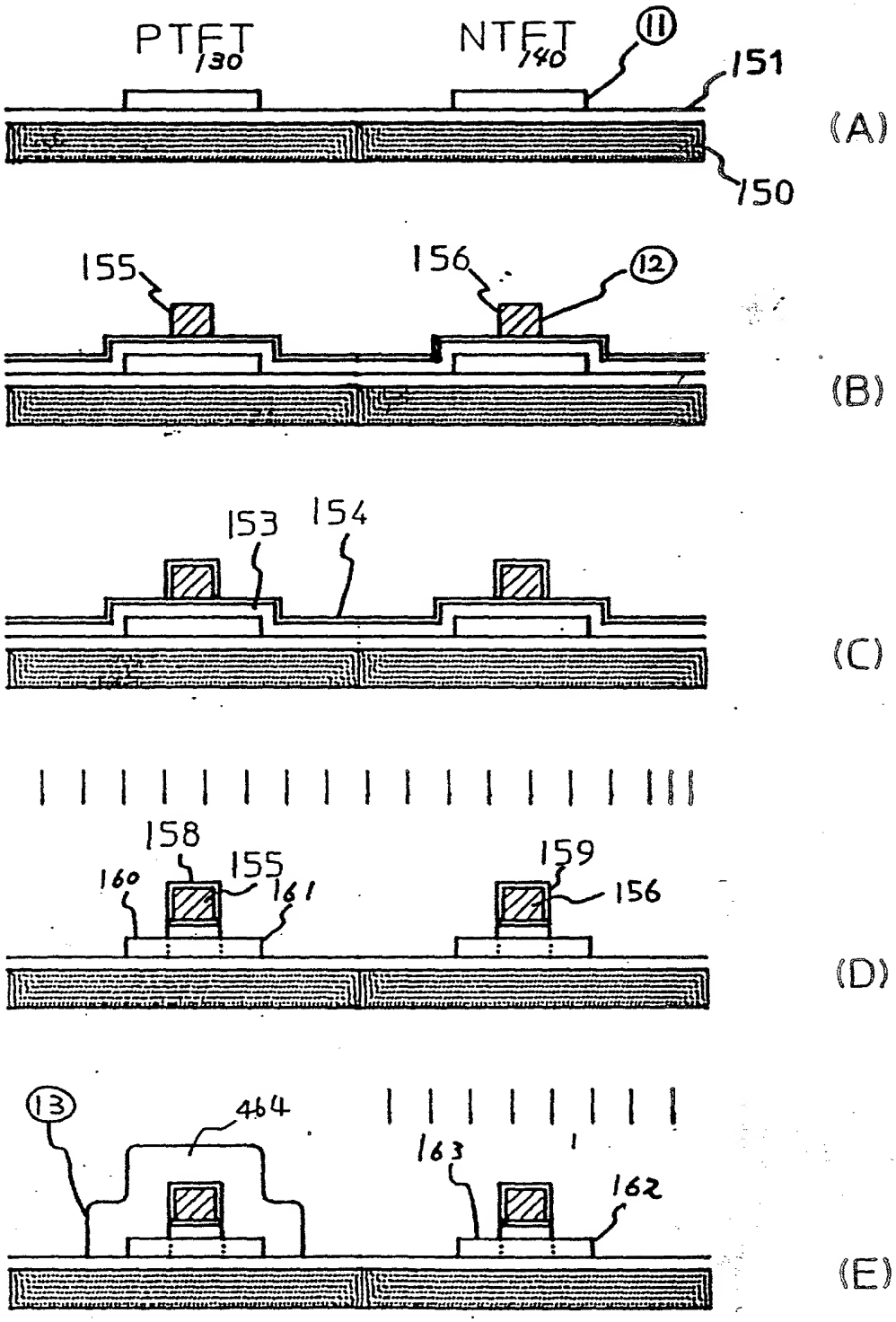
VSS'
175

Fig. 11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(D)
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464
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162
(E)

Fig. 11

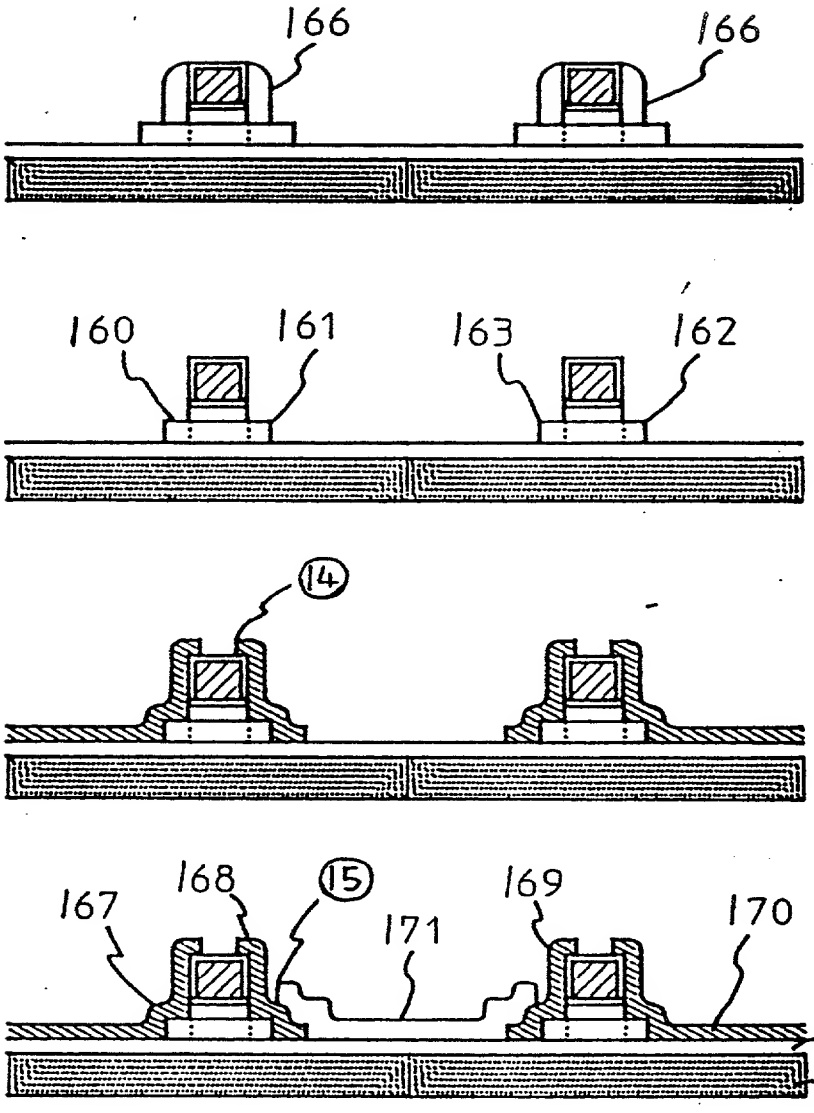

Fig. 12

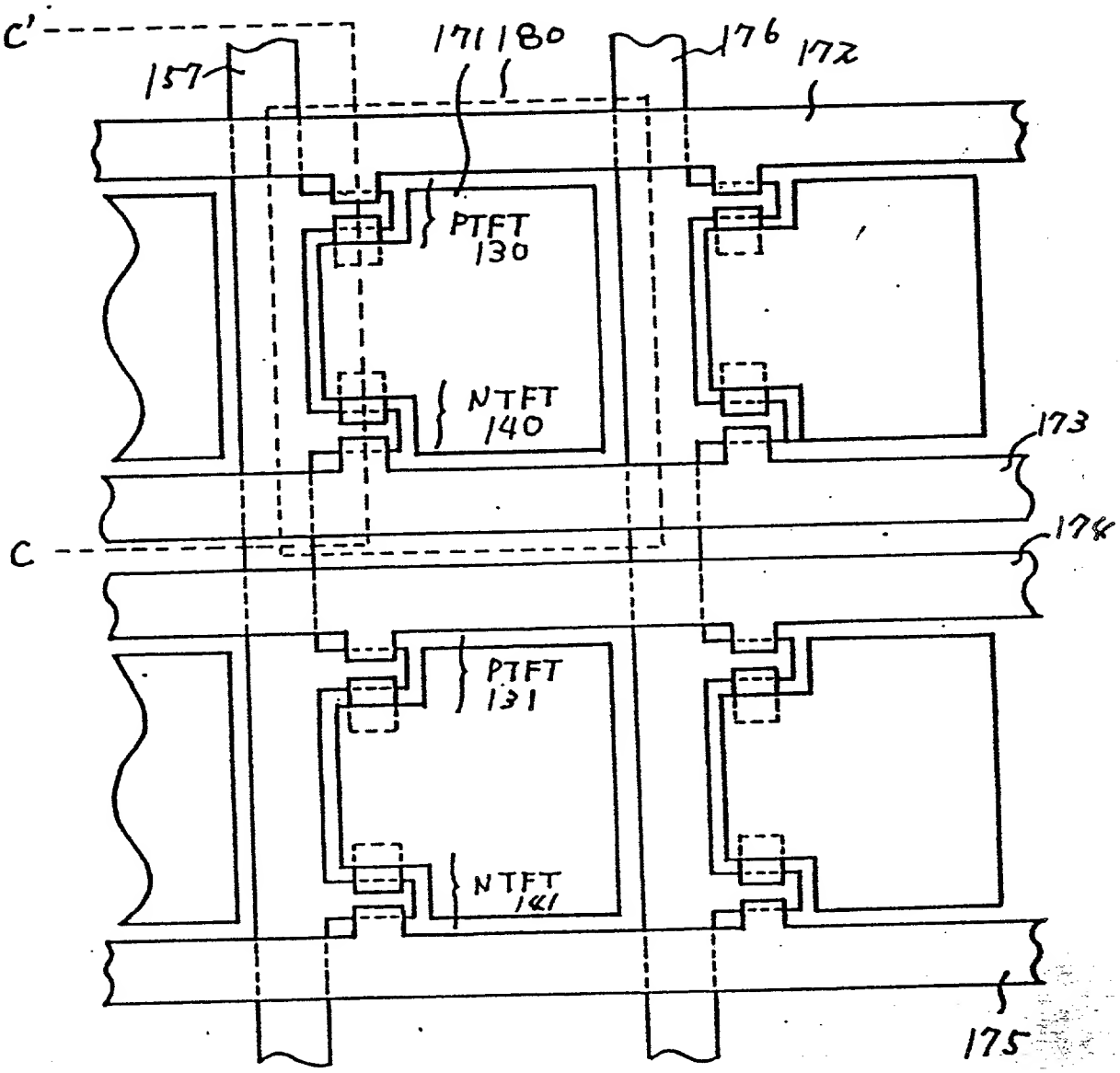
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Fig. 13

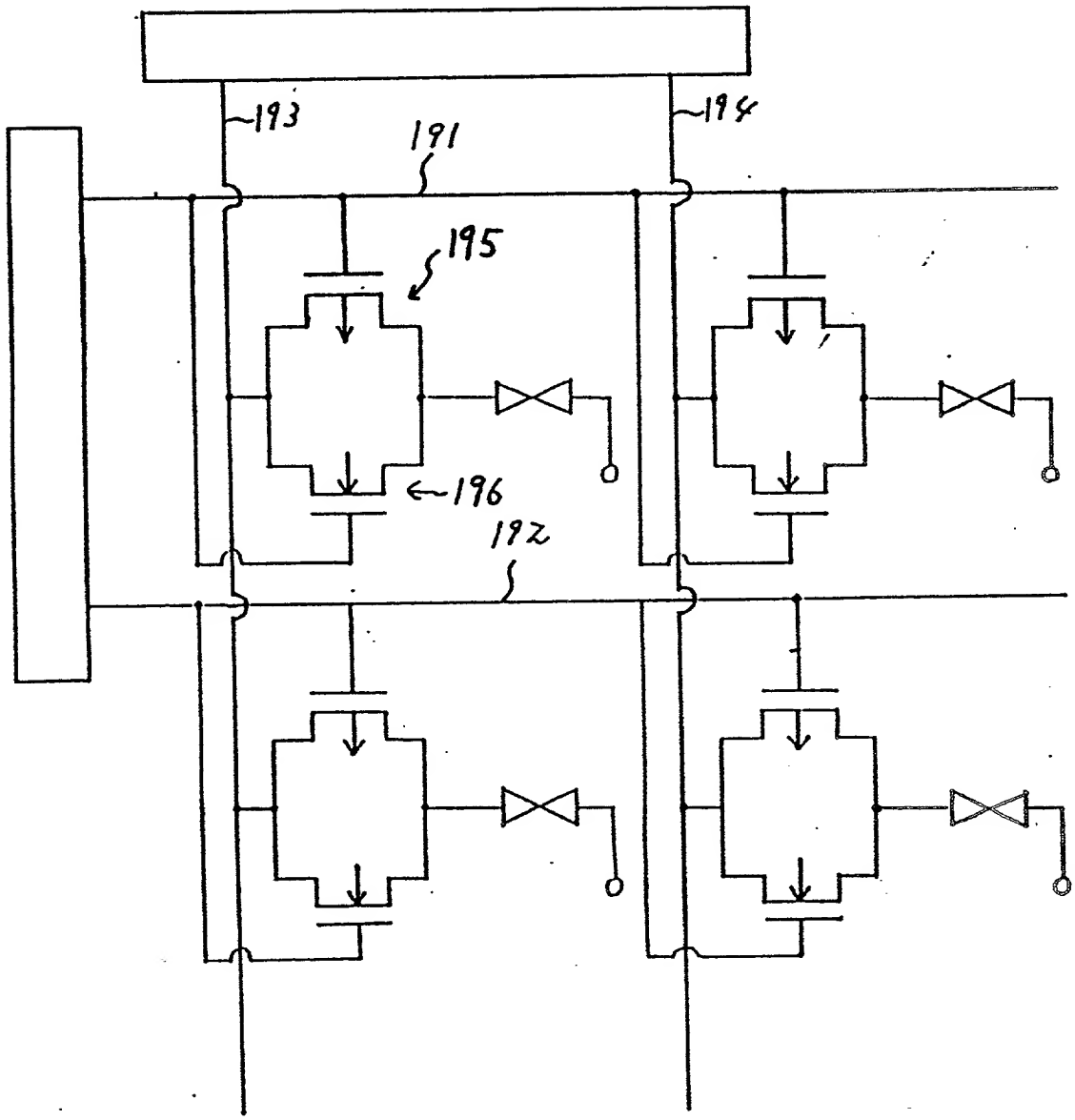
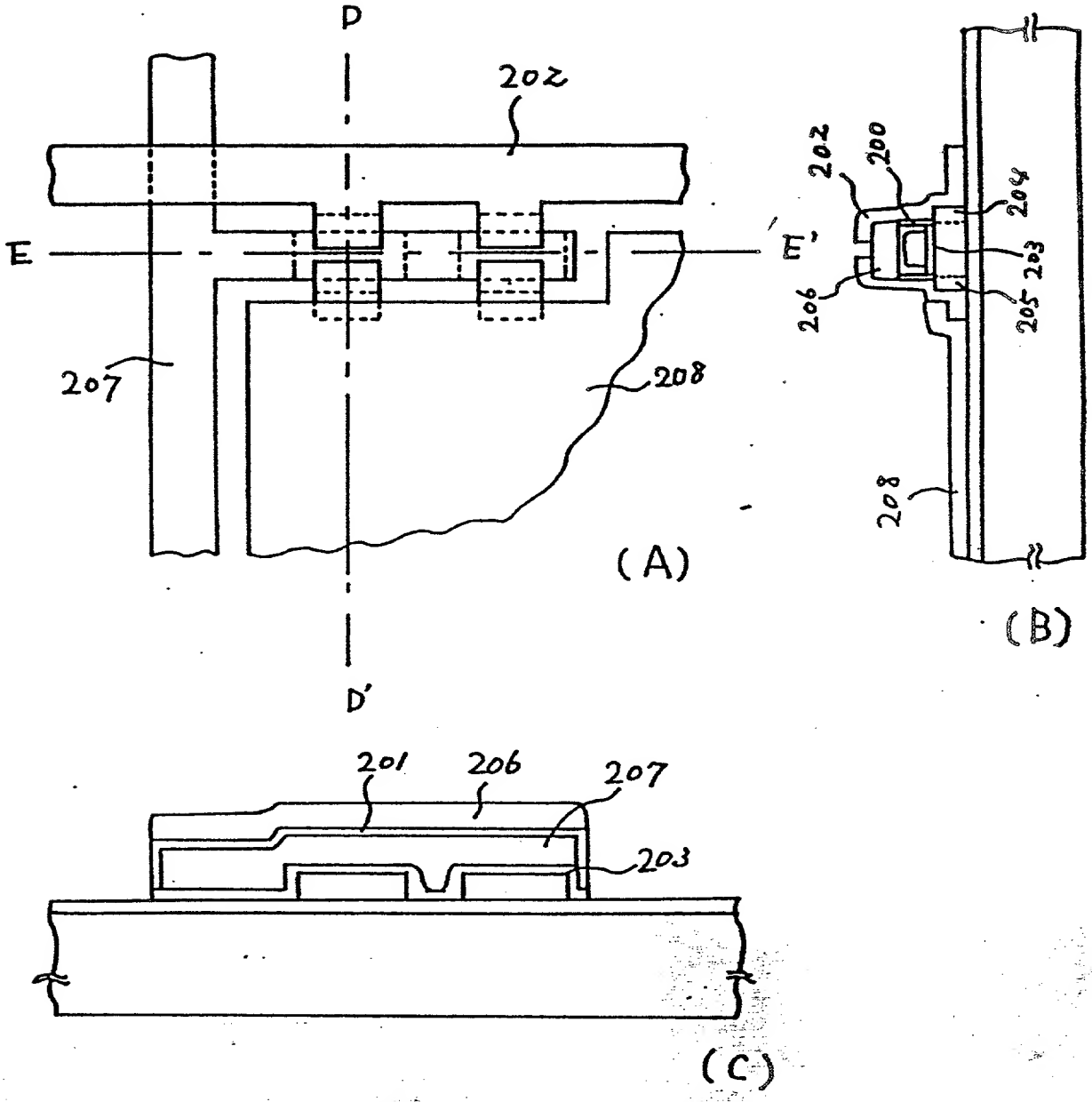


Fig. 14



DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO.
6756-704

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: * SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME

Insert Title

, the specification of which is attached hereto unless the following box is checked:

Check Box If Appropriate — For Use Without Specification Attached

☐ The specification was filed on _____
and was assigned Serial No. _____ (if known)
and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Prior Foreign Application(s)

Priority Claimed

Insert Priority Information (If appropriate)

(Number)	(Country)	(Month/Day/Year Filed)	Yes	No
3-65418	JAPAN	March 6, 1991	☒	☐
3-135569	JAPAN	May 11, 1991	☒	☐
			☐	☐
			☐	☐
			☐	☐

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months Prior To The Filing Date of This Application:

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status — patented, pending, abandoned)

(Application Serial No.) (Filing Date) (Status — patented, pending, abandoned)

Revised 11/90

*NOTE: Must be completed.

I hereby appoint the following attorneys to prosecute this application and/or an international application and to transact all business in the Patent and Trademark Office connected therewith:

Daniel W. Sixbey (Reg. No. 20,932)	Gerald J. Ferguson, Jr. (Reg. No. 23,016)
Stuart J. Friedman (Reg. No. 24,312)	David S. Safran (Reg. No. 27,997)
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Insert Name of Non-U.S. firm, attorney or agent

The undersigned hereby authorize any U. S. attorney or agent named herein to accept and follow instructions from ____________________ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

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	RESIDENCE (City, State & Country):	CITIZENSHIP:	
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country):		